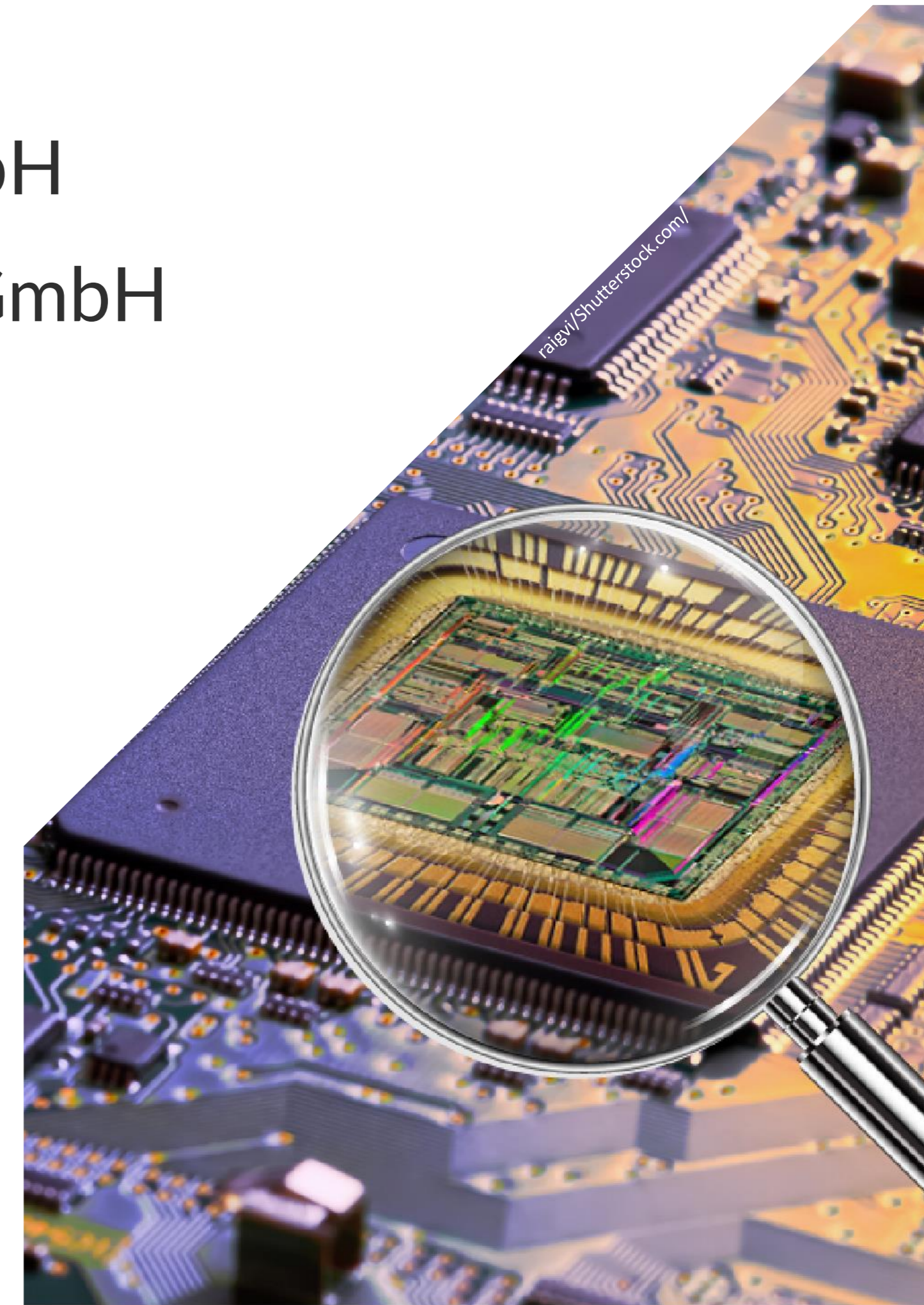


Structural High-level Tests

Alexander Weiss, Accemic Technologies GmbH

Martin Heining, HEICON Global Engineering GmbH



ACCEMIC
TECHNOLOGIES

The pioneer in embedded systems dynamic analysis.
Automated, non-intrusive and continuous.

Motivation

Bug-free Software is a Myth.

Trends:

- More complex integrated systems
- Software-driven safety-critical applications (e.g. autonomous driving)
- Increased number of critical software defects

Software defects are a considerable cause for

- Project **schedule overruns** (~60%)¹
- Project **budget overruns** (~50%)¹
- Project **cancellation** (~10-20%)^{2,3}
- Higher **maintenance costs**
(Airbus study⁴: Cost of a non-frequent failure: up to 500,000 €)
- **Injuries, accidents, recalls**

Toyota "Unintended Acceleration" Has Killed 89



A 2009 Toyota Prius, which was in an accident, is seen at a police station in Hammon, New York, Wednesday, March 10, 2010. The driver of the Toyota Prius told police that the car accelerated on its own, then lurched down a driveway, across a road and into a stone wall. (AP Photo/Seth Weng) AP PHOTO/SETH WENG

Unintended acceleration in Toyota vehicles may have been involved in the deaths of 89 people over the past decade, upgrading the number of deaths possibly linked to the massive recalls, the government said Tuesday.

The National Highway Traffic Safety Administration said that from 2000 to mid-May, it had received more than 6,200 complaints involving sudden acceleration in Toyota vehicles. The reports include 89 deaths and 57 injuries over the same period. Previously, 52 deaths had been suspected of being connected to the problem. <http://www.cbsnews.com/news/toyota-unintended-acceleration-has-killed-89/>
© Copyright 2014, Philip Koopman. CC Attribution 4.0 International license.

¹ Gartner Research

² Emam et al, "A Replicated Survey of IT Software Project Failures."

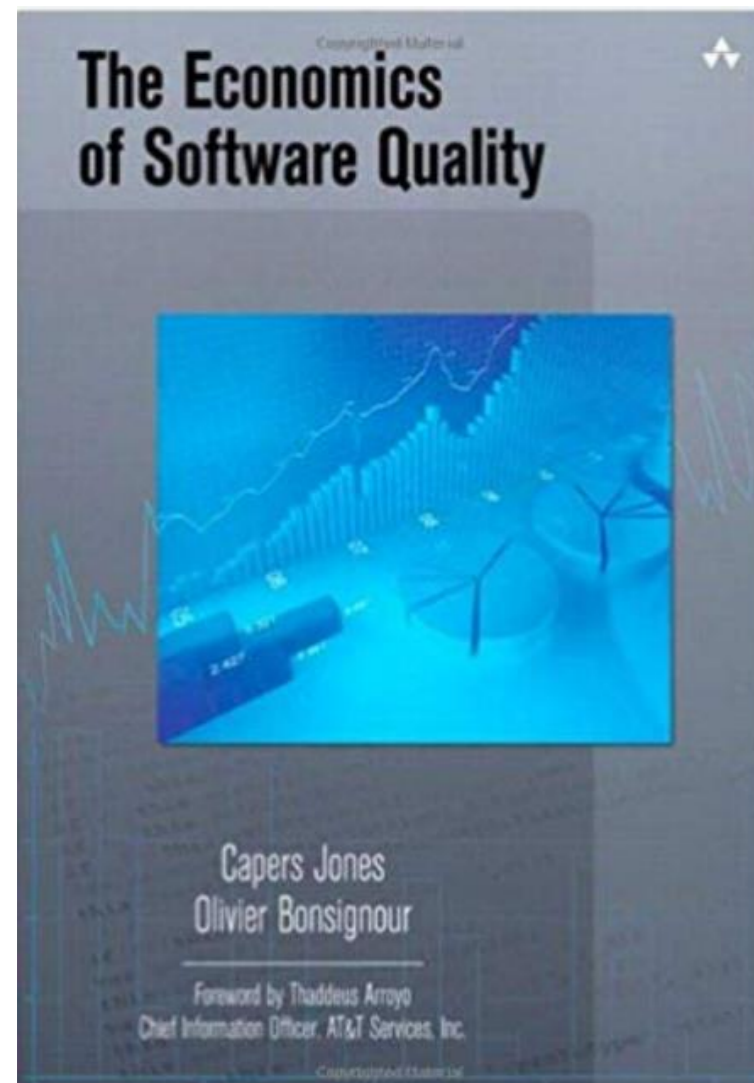
³ Standish Chaos Report

⁴ Hanke et al, "Assessment of multi-core integration infrastructure" Munich, 2014.

Motivation

Bug-free Software is a Myth.

McKinsey & Company (2018):
"Snowballing complexity is causing significant software-related quality issues ..."



Size of SW projects in FP	Average Defect Potential (Defects / FP)	Defect Removal Efficiency
100	3,00	98%
10.000	6,25	96%
1.000.000	8,25	86%

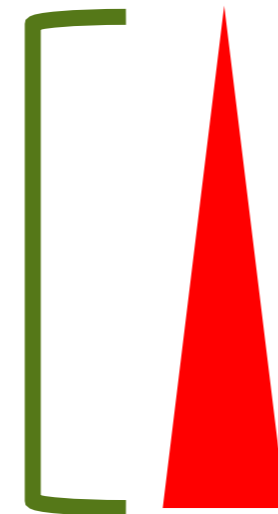
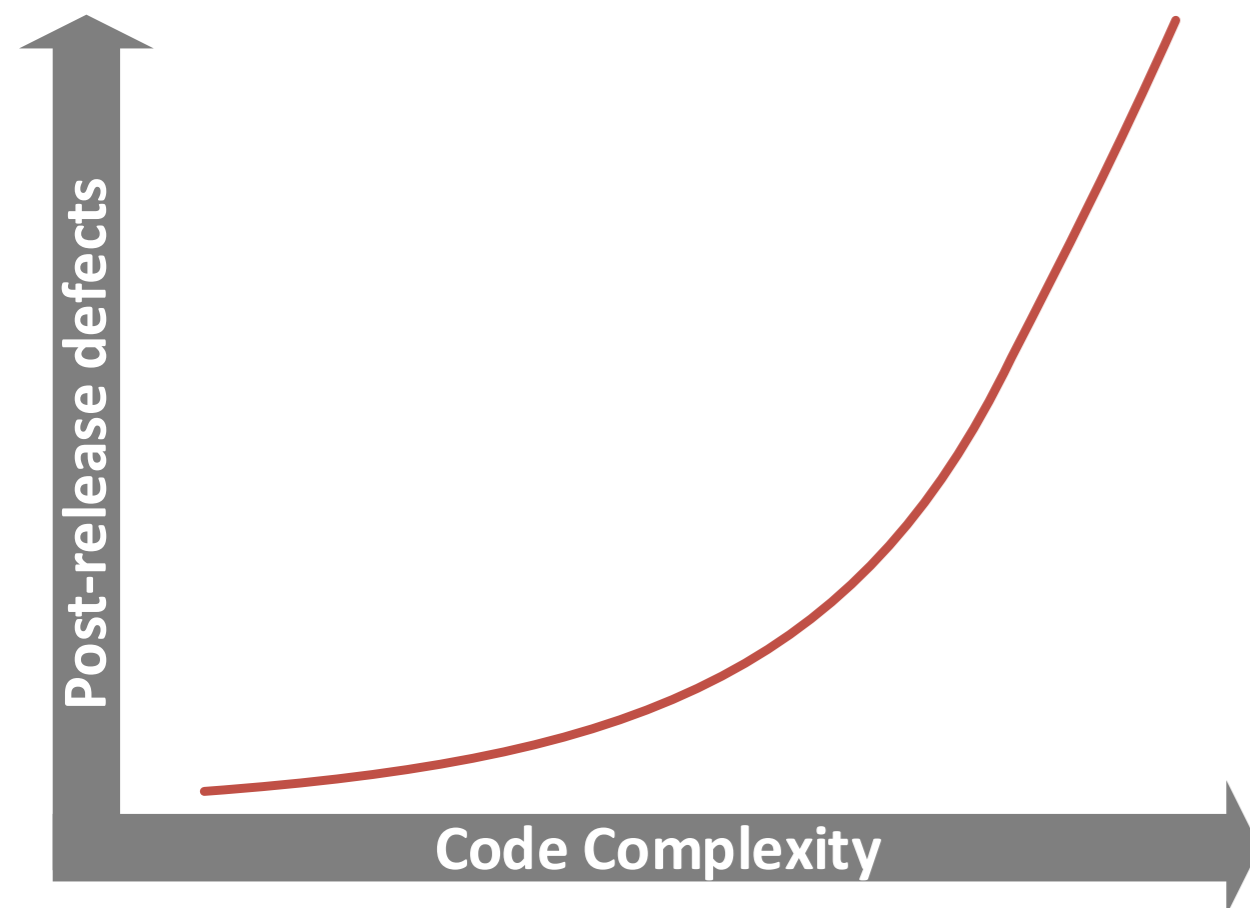
1 MLOC (C-Code) => 6.250 FP => ~35.000 defects => ~ 2.500 Post Release Defects

* 1 FP (Function Point): ~160 LOC (C language), ~64 LOC (ADA), ~32 LOC (C++)

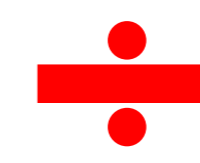
Motivation

Bug-free Software is a Myth.

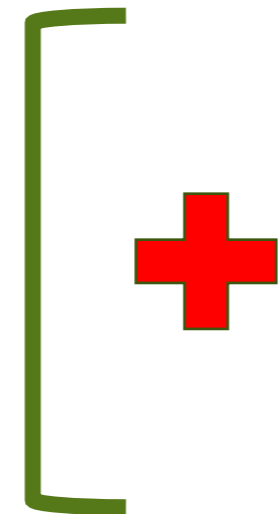
Increasing size
of SW projects



Average Defect Potential increases with the size of SW projects.



Defect Removal Efficiency decreases with the size of SW projects.



Additional non-deterministic defects, caused by multicore interferences



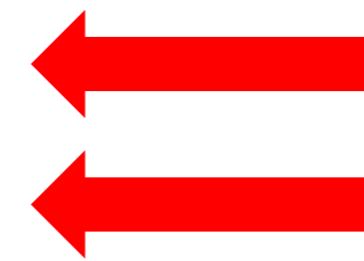
- Challenges for embedded software architecture
- Challenges for testing
- Challenges for maintenance



What we can do

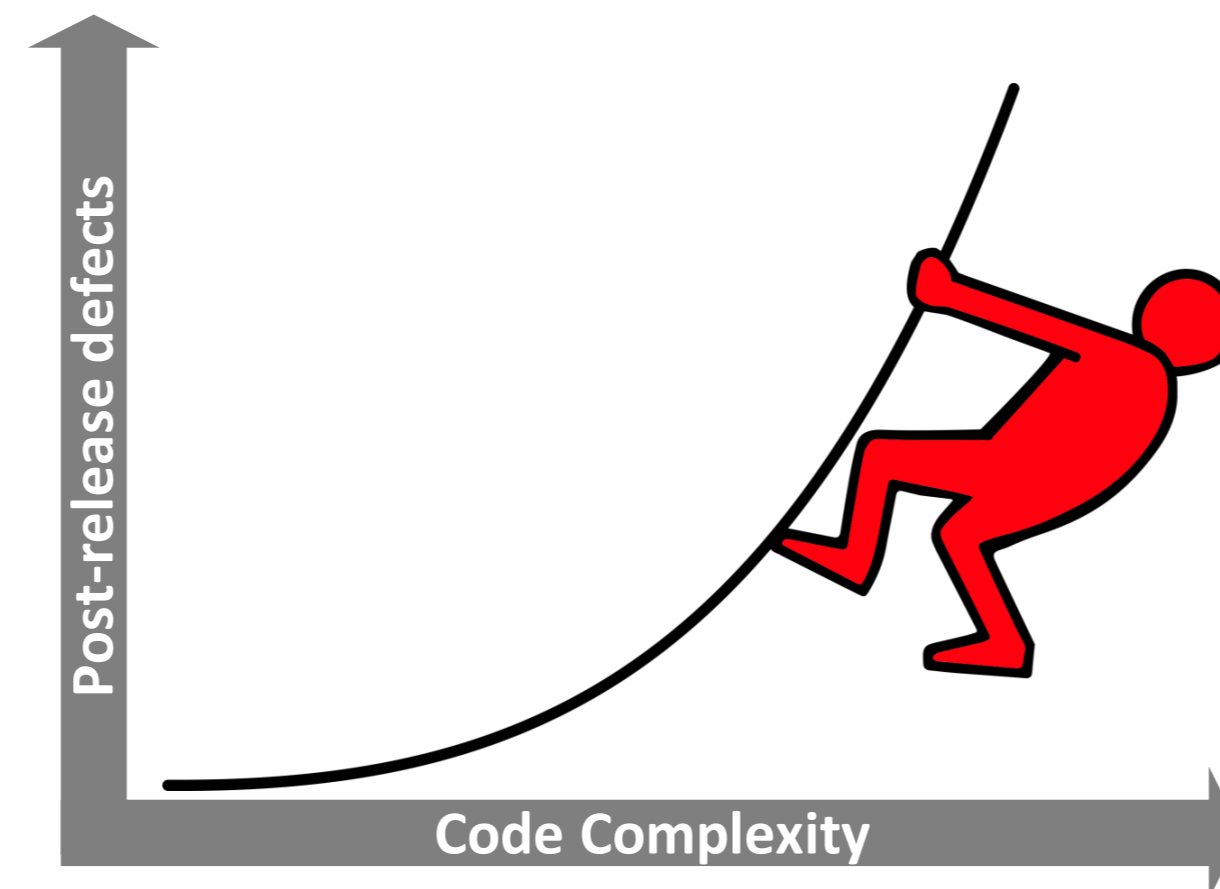
Challenges:

- Improve development process
- Improve test effectiveness and test efficiency
- Improve in-field analysis and debug capabilities
-



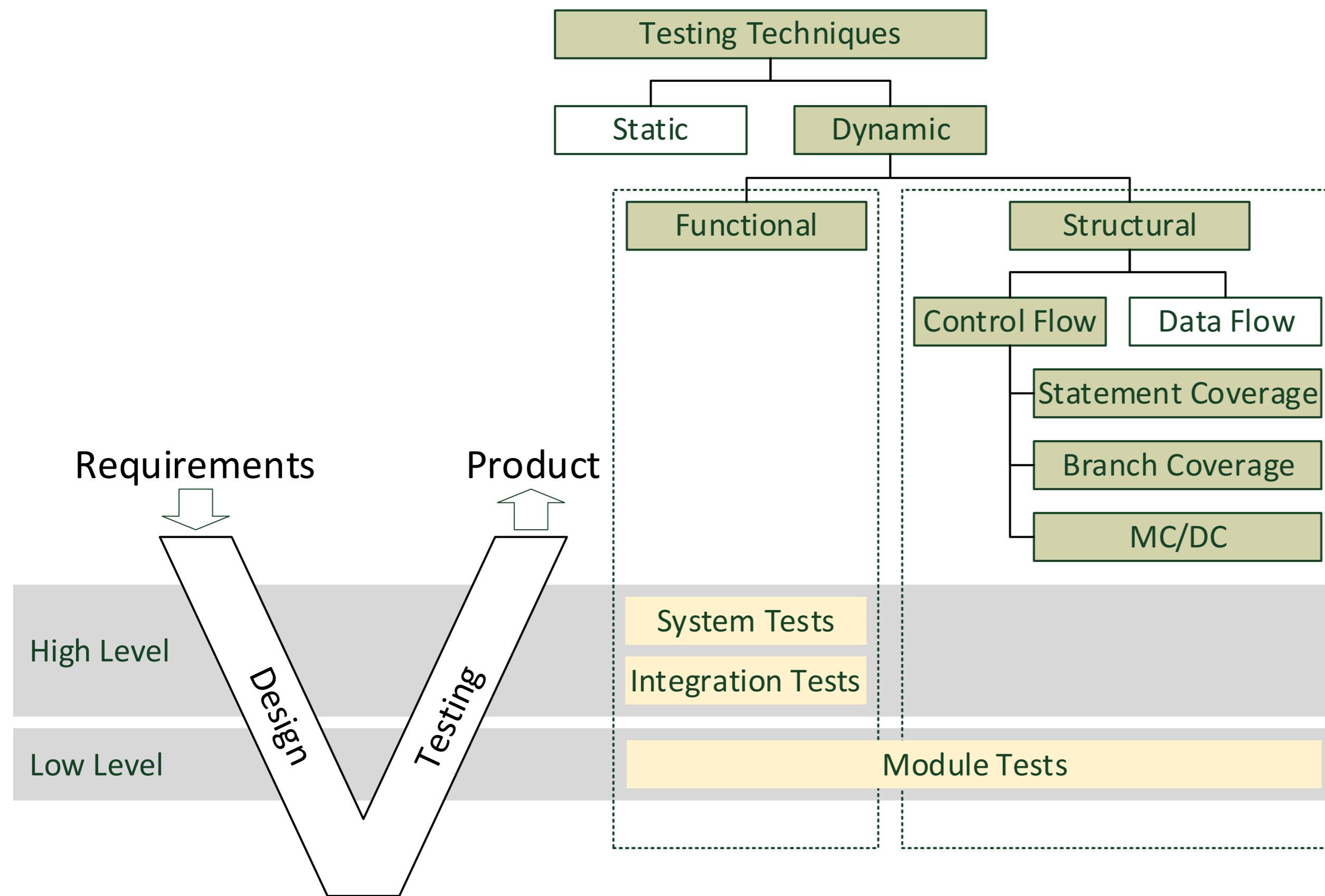
Our contribution:

- Regain observation capabilities in highly integrated multicore systems
- Enable continuous, non-intrusive online observation and automated validation
 - Structural coverage at higher test levels
 - Timing analysis at higher test levels



Dynamic Tests

Overview



Functional tests (black box)

Test the implementation of the functional requirements.

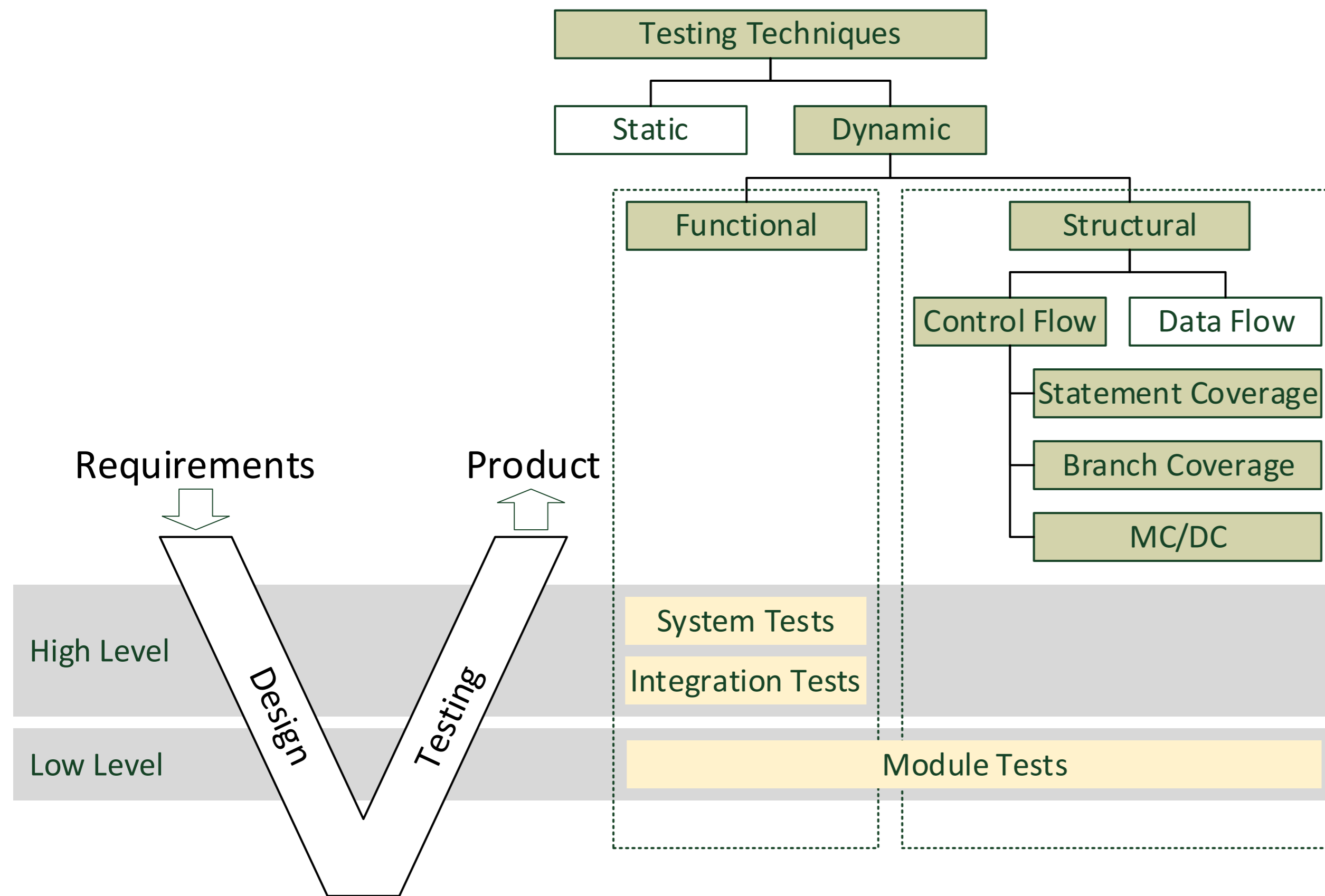
Structural tests (white box)

Did my functional tests use all my code?



Dynamic Tests

Overview



Functional tests

Test the implementation of the functional requirements.

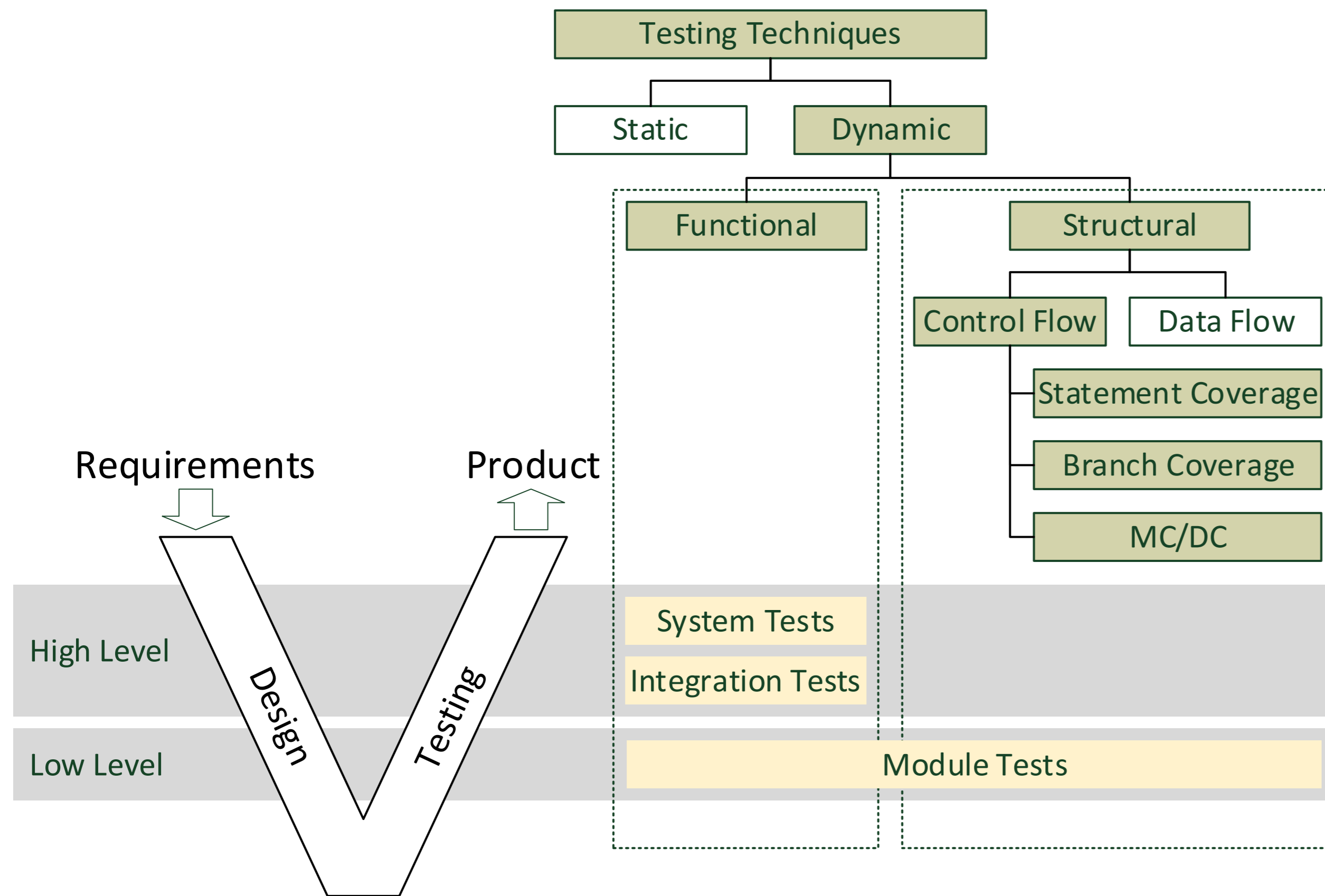
Structural tests

Did my functional tests use all my code?



Dynamic Tests

Overview

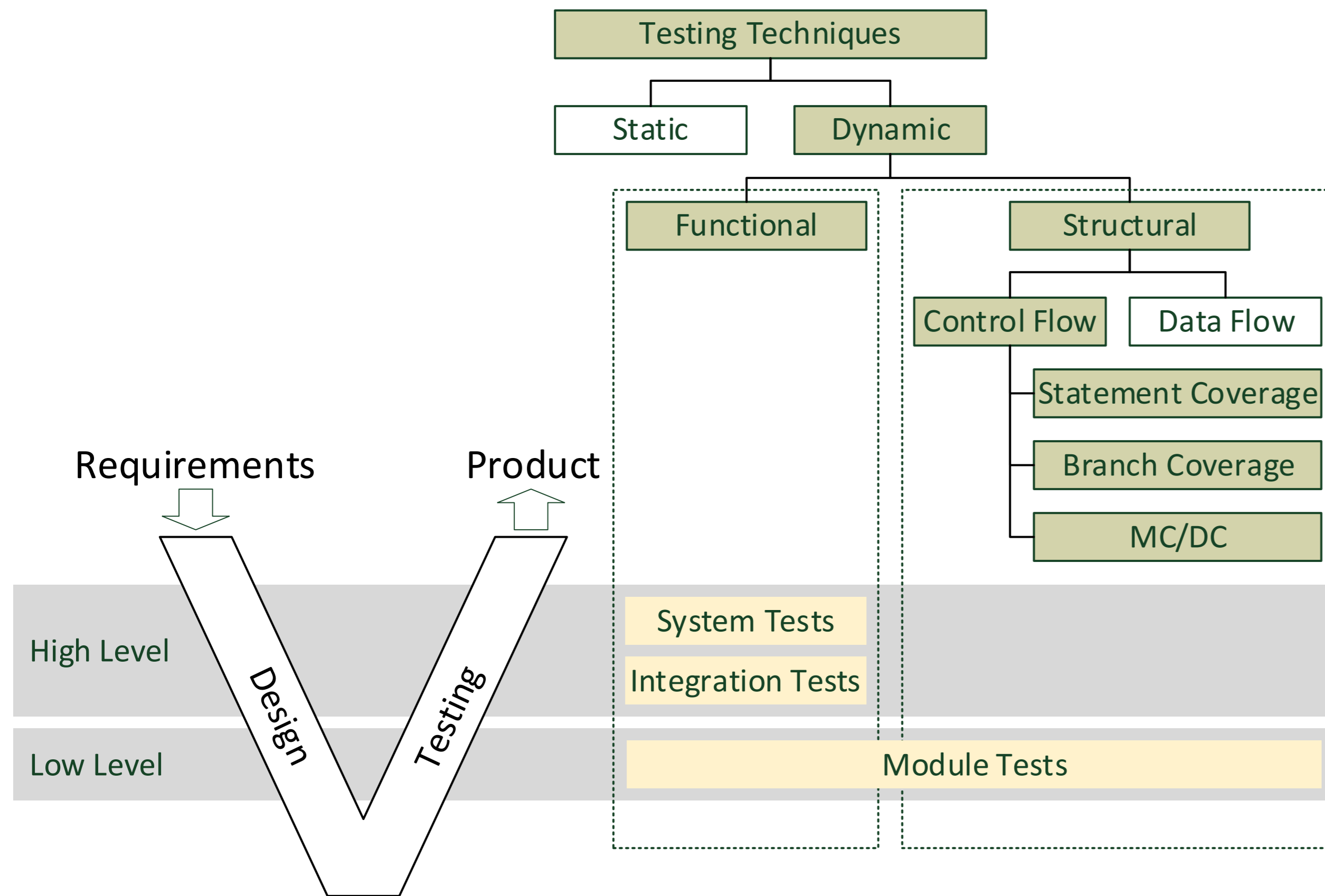


$$\text{Statement Coverage} = \frac{\# \text{ of Executed Statements}}{\# \text{ of Statements}}$$



Dynamic Tests

Overview

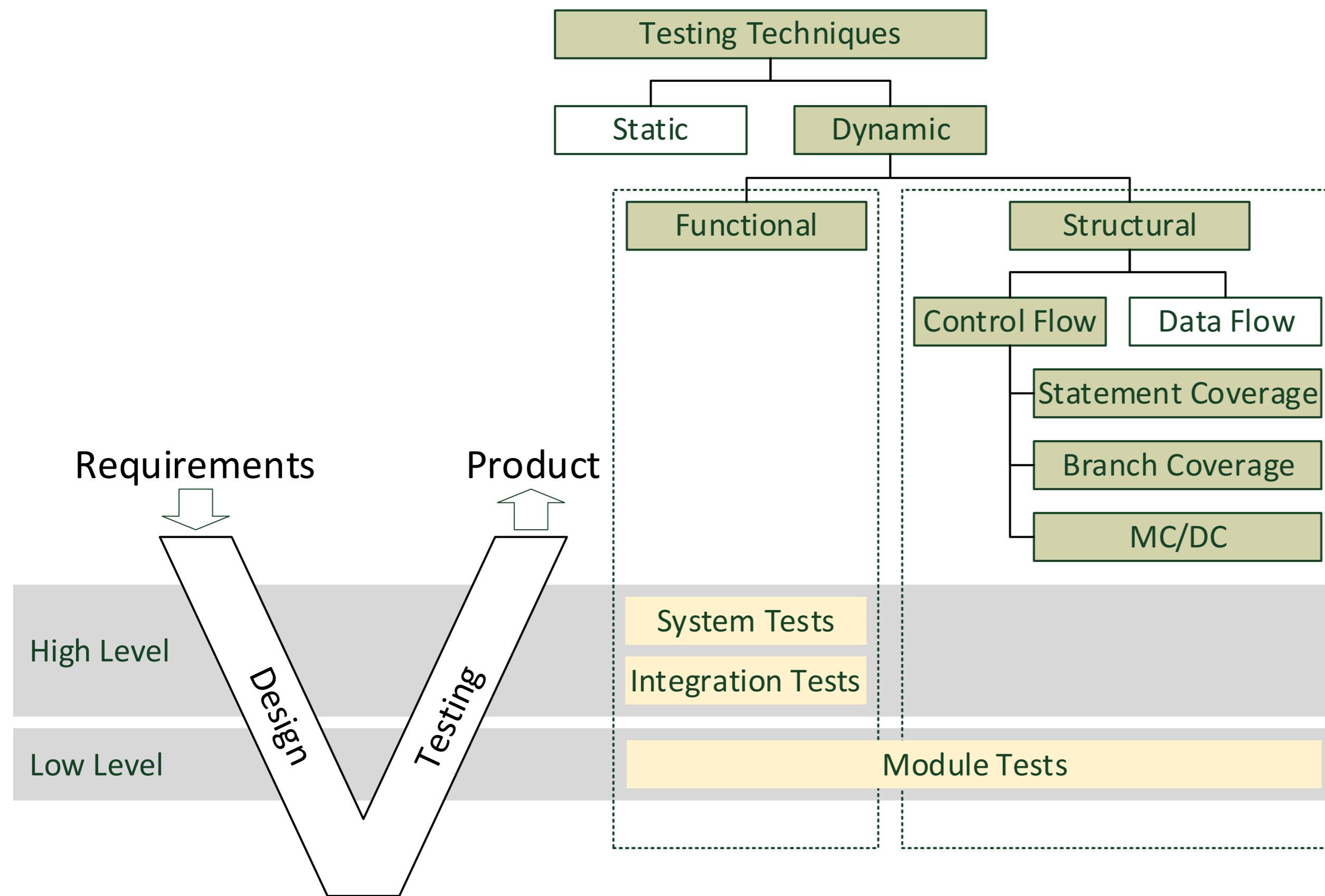


$$\text{Branch Coverage} = \frac{\# \text{ of Executed Branches}}{\# \text{ of Branches}}$$



Dynamic Tests

Overview



A Practical Tutorial on Modified Condition/ Decision Coverage

MC/DC

Each condition in a decision has been shown to independently affect that decision's outcome.

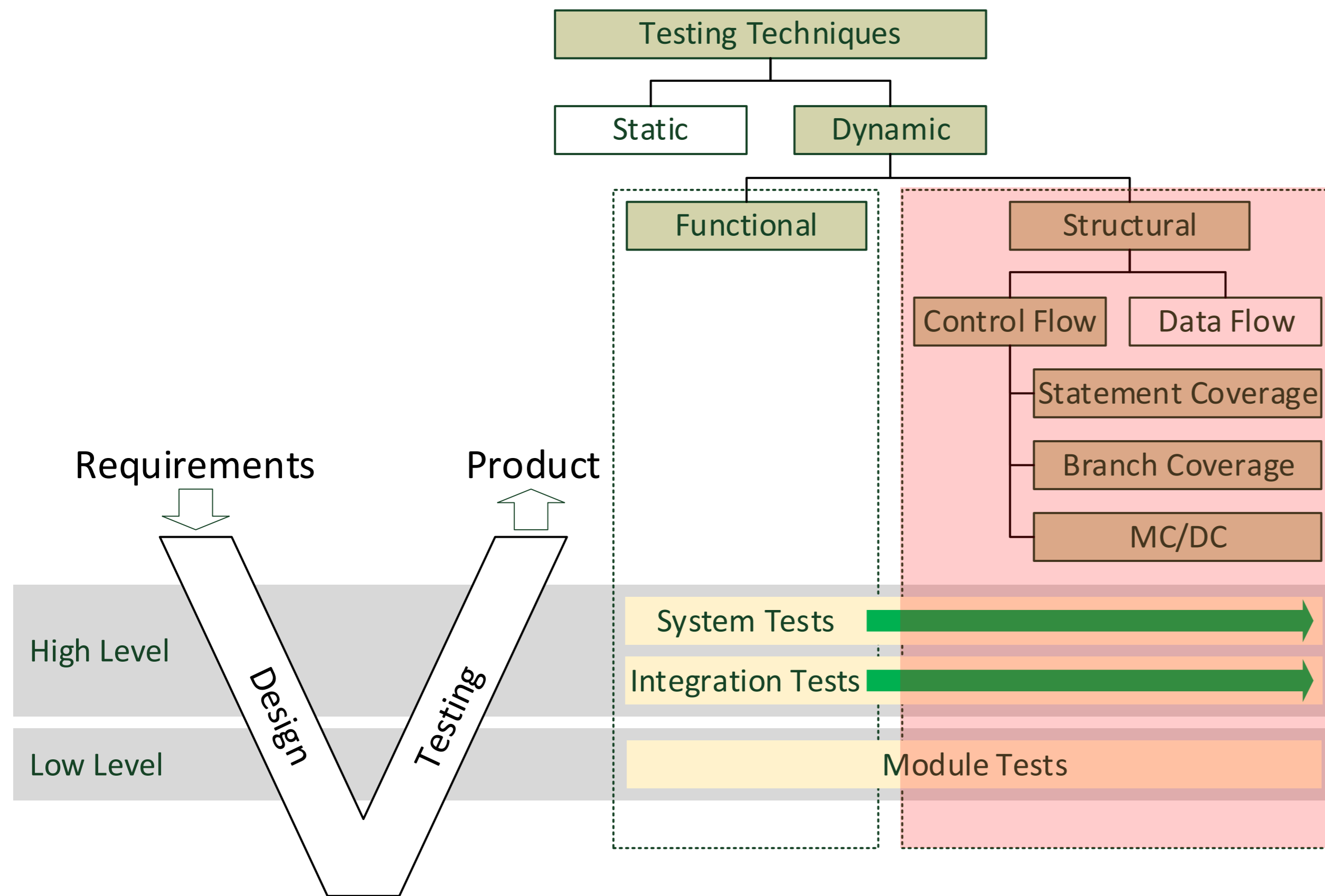
A condition is shown to independently affect a decision's outcome by varying just that condition while holding fixed all other possible conditions.

<https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20010057789.pdf>



Dynamic Tests

Overview



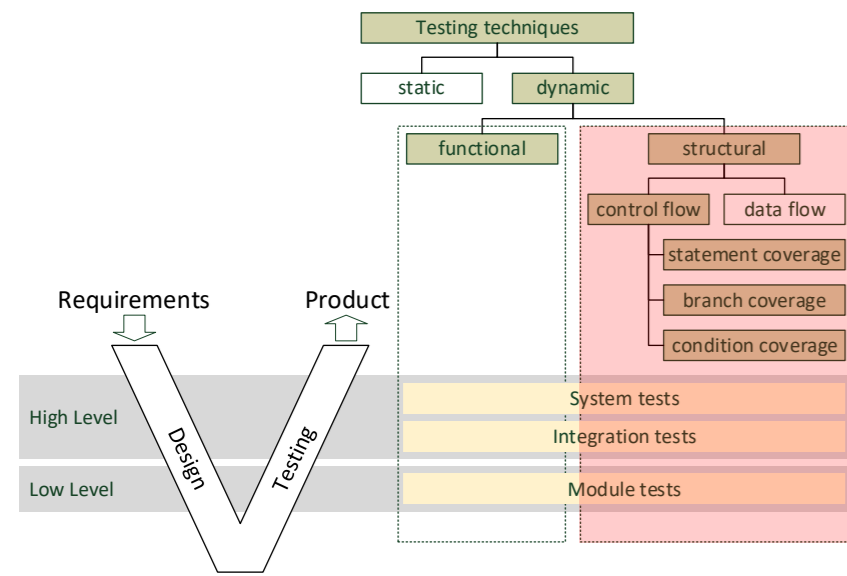
Functional tests (black box)
Test the implementation of the functional requirements.

Structural tests (white box)
Did my functional tests use all my code?

IMPROVEMENT:
Structural tests for high-level tests.



High-level Structural Tests

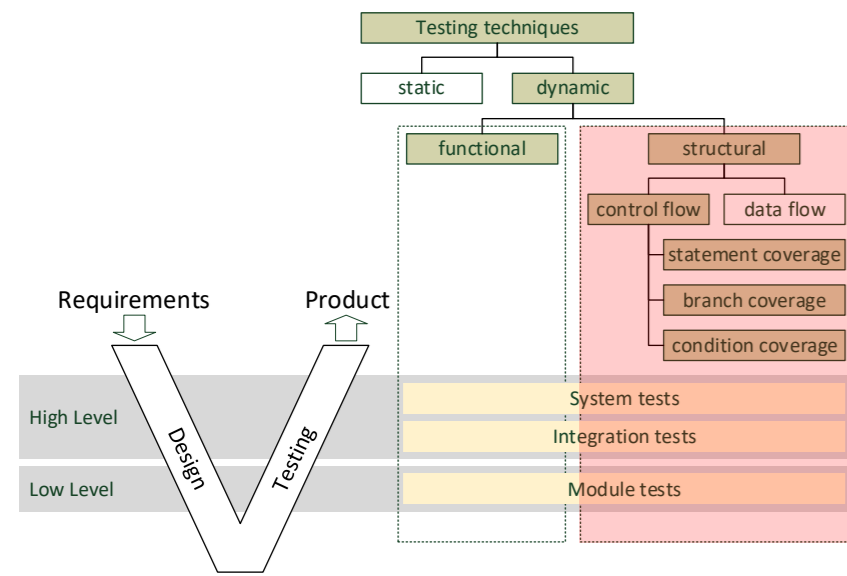


Requirements für structural tests

	Long observation	No change of timing behavior	No change of memory footprint	
System tests	Y	Y	Y	Limitations by using SW instrumentation
Integration tests	Y	Y	Y	Limitations by using SW instrumentation
Module tests	N	N	N	SW instrumentation is perfect.



High-level Structural Tests

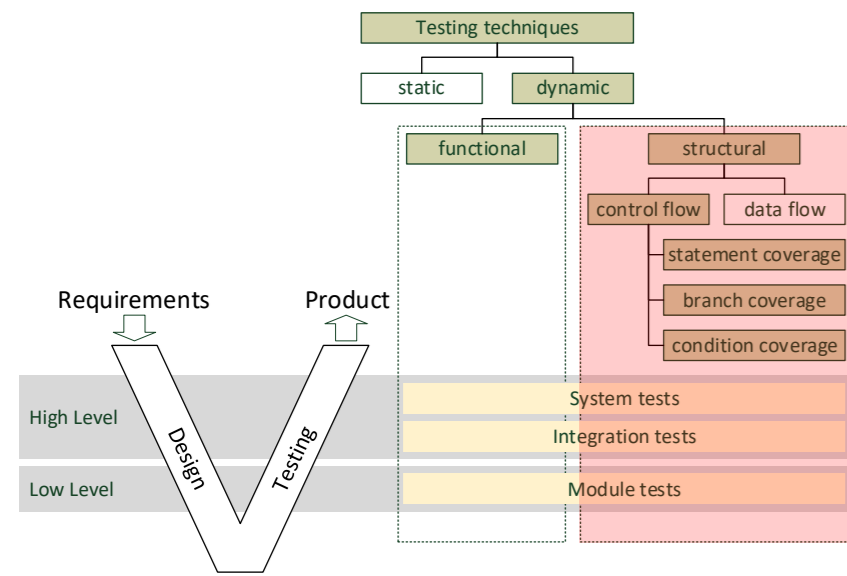


Requirements für structural tests

	Long observation	No change of timing behavior	No change of memory footprint	
System tests	Y	Y	Y	Limitations by using SW instrumentation
Integration tests	Y	Y	Y	Limitations by using SW instrumentation
Module tests	N	N	N	SW instrumentation is perfect.

State of the art:
Measuring code coverage
using SW instrumentation

High-level Structural Tests

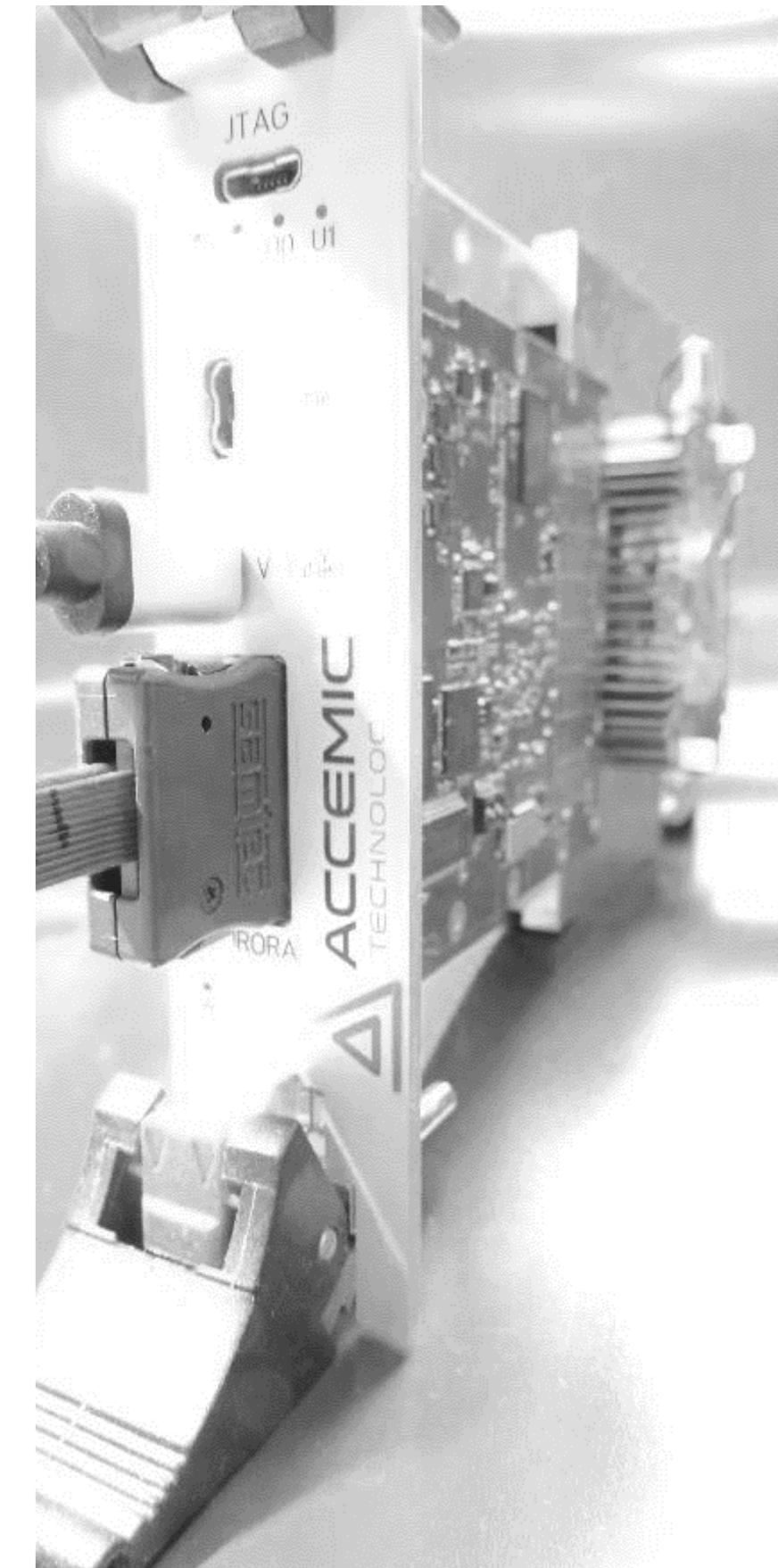
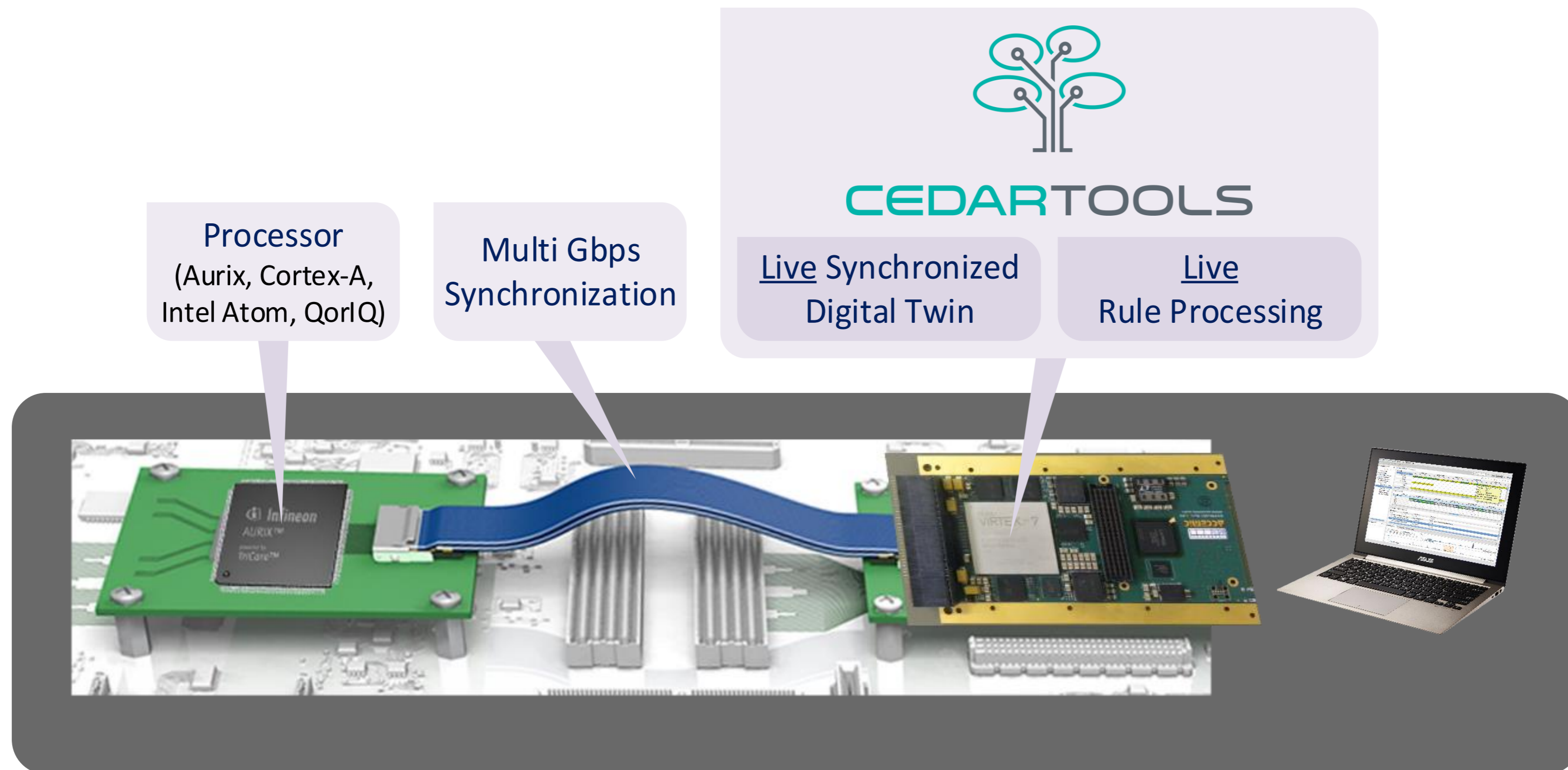


Requirements für structural tests

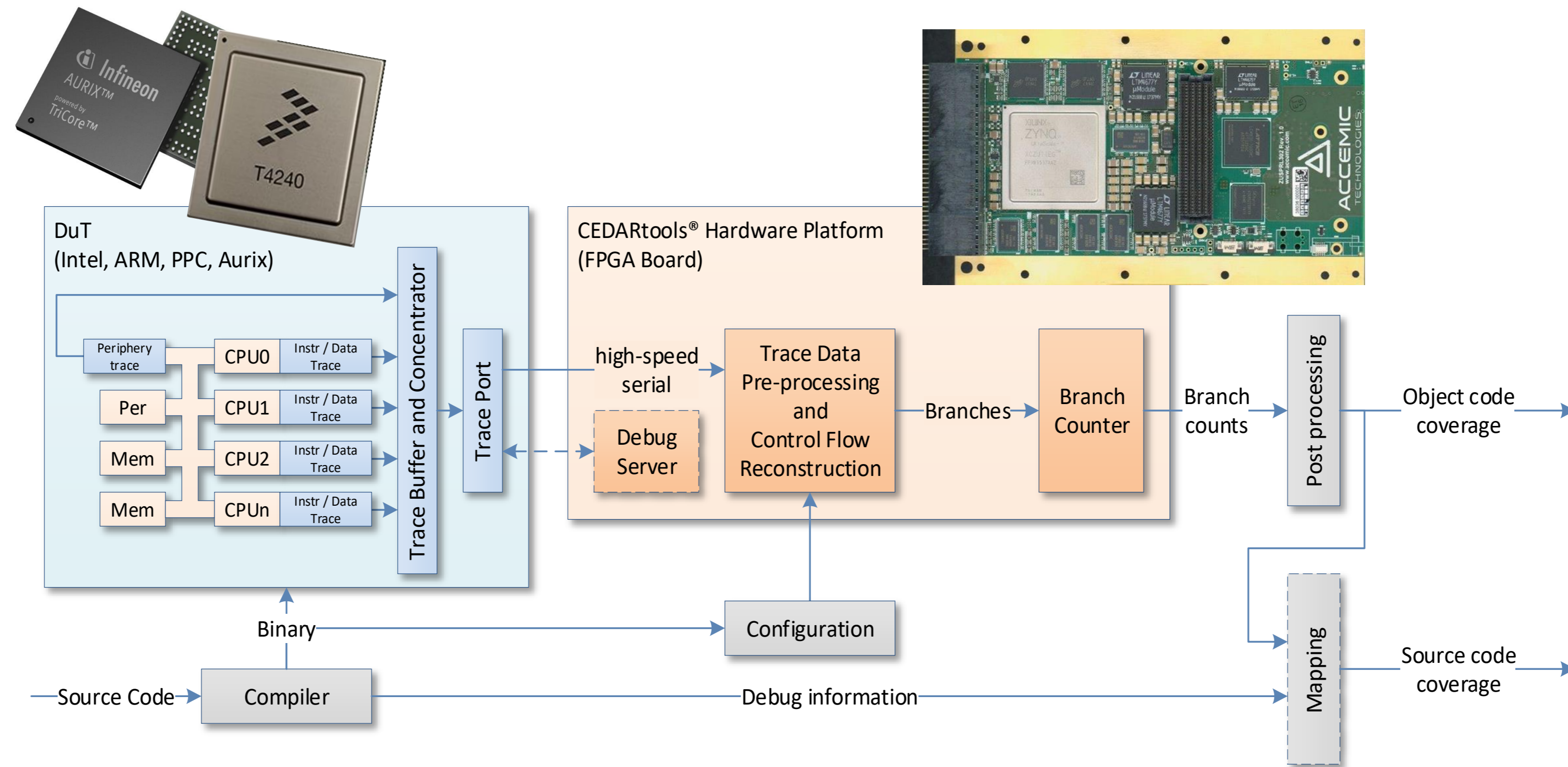
	Long observation	No change of timing behavior	No change of memory footprint	
System tests	Y	Y	Y	Limitations by using SW instrumentation
Integration tests	Y	Y	Y	Limitations by using SW instrumentation
Module tests	N	N	N	SW instrumentation is perfect.

New approach:
Non-intrusive and continuous observation

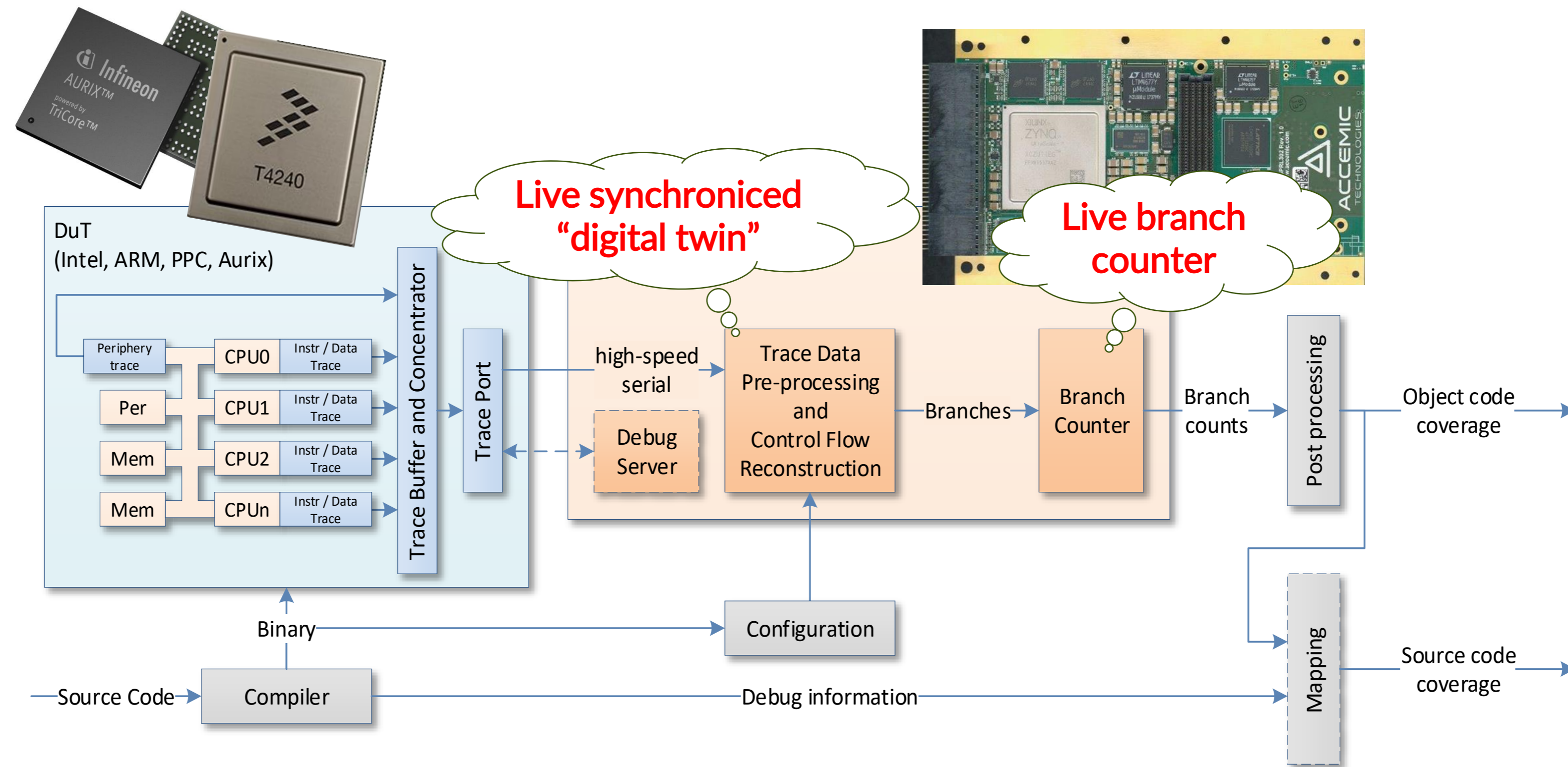
Non-intrusive and Continuous Observation



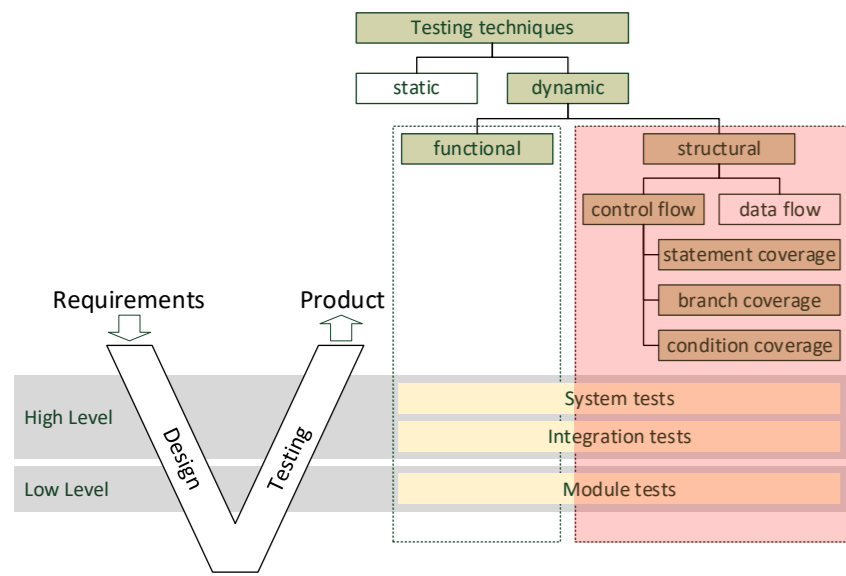
Non-intrusive and Continuous Observation



Non-intrusive and Continuous Observation



High-level Structural Tests



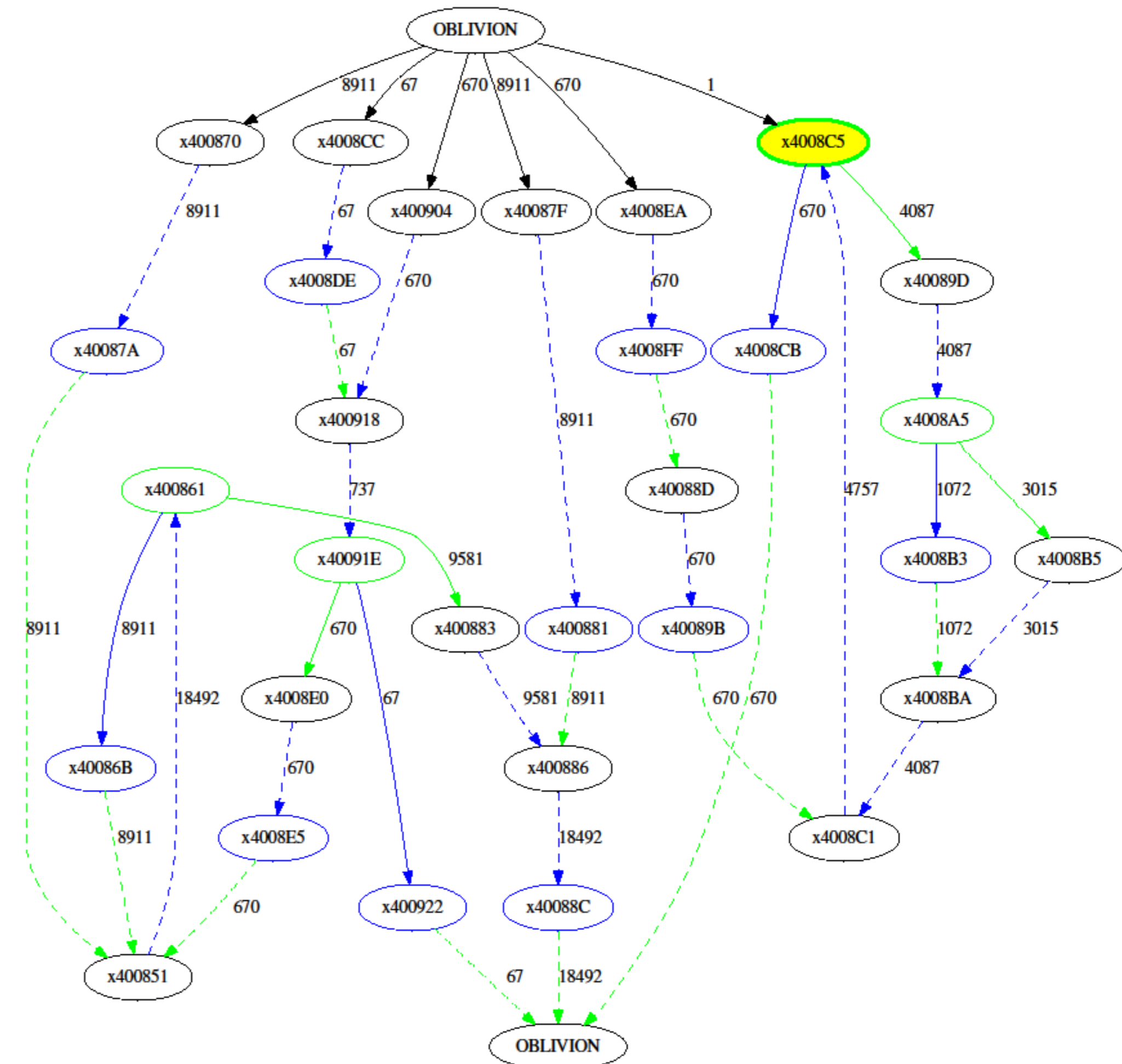
Continuous and non-intrusive

- Statement Coverage
- Branch Coverage (EX/NEX)
- Performance measurement (count executed instructions)

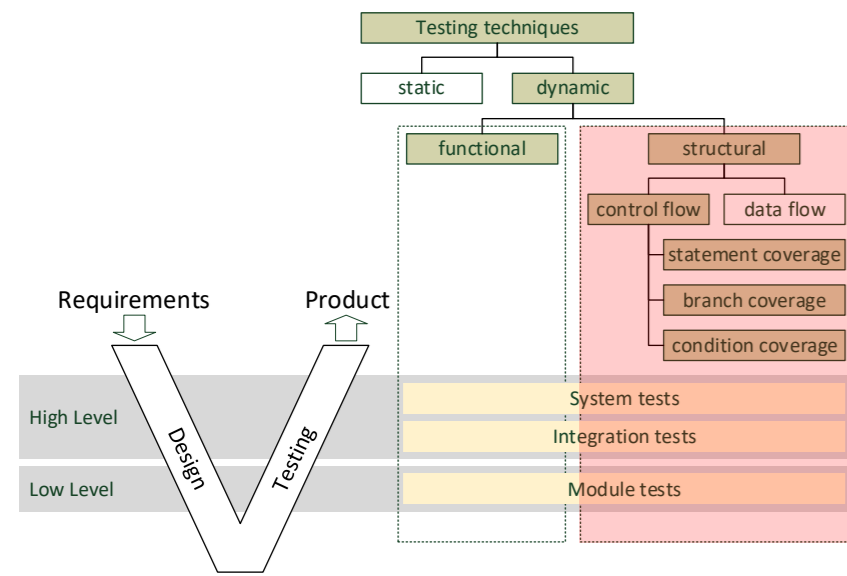
- Measured on object code level
- Measured on release code
- No instrumentation
- No limitation due to trace buffer size

Targets:

- Infineon Aurix™ (TC2xx & TC3xx),
- Arm® Cortex® -A9,
- Intel® x86 (Atom® E3950),
- NXP QorIQ® P- and T-series,
- Arm® Cortex® -A5x under development.



High-level Structural Tests



Continuous and non-intrusive

- Statement Coverage
- Branch Coverage (EX/NEX)
- Performance measurement (count executed instructions)

- Measured on object code level
- Measured on release code
- No instrumentation
- No limitation due to trace buffer size

Targets:

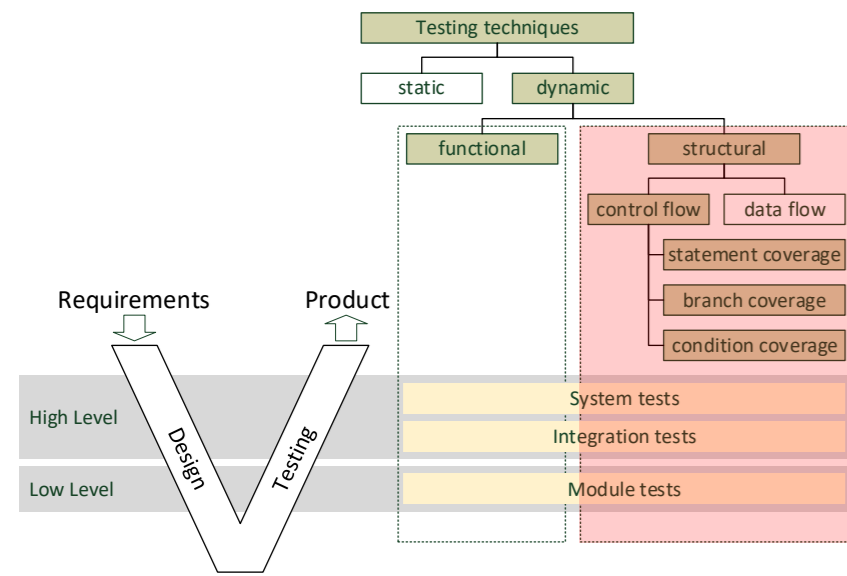
- Infineon Aurix™ (TC2xx & TC3xx),
- Arm® Cortex® -A9,
- Intel® x86 (Atom® E3950),
- NXP QorIQ® P- and T-series,
- Arm® Cortex® -A5x under development.

	70	10062C: e51b3010 ldr r3, [fp, #-16]
	70	100630: e3530001 cmp r3, #1
[+,+]	70	100634: 9a000010 bls 10067c <_Z13collatz_depthj+0x68>
	61	100678: eaffffeb b 10062c <_Z13collatz_depthj+0x18>

	61	100638: e51b3010 ldr r3, [fp, #-16]
	61	10063C: e2033001 and r3, r3, #1
	61	100640: e3530000 cmp r3, #0
[+,+]	61	100644: 0a000005 beq 100660 <_Z13collatz_depthj+0x4c>
	16	100648: e51b2010 ldr r2, [fp, #-16]
	16	10064C: e1a03002 mov r3, r2
	16	100650: e1a03083 lsl r3, r3, #1
	16	100654: e0833002 add r3, r3, r2
	16	100658: e2833001 add r3, r3, #1
	16	10065C: ea000001 b 100668 <_Z13collatz_depthj+0x54>
	45	100660: e51b3010 ldr r3, [fp, #-16]
	45	100664: e1a030a3 lsr r3, r3, #1
	61	100668: e50b3010 str r3, [fp, #-16]



High-level Structural Tests



Continuous and non-intrusive

- Statement Coverage
- Branch Coverage (EX/NEX)
- Performance measurement (count executed instructions)

- Measured on object code level
- Measured on release code
- No instrumentation
- No limitation due to trace buffer size

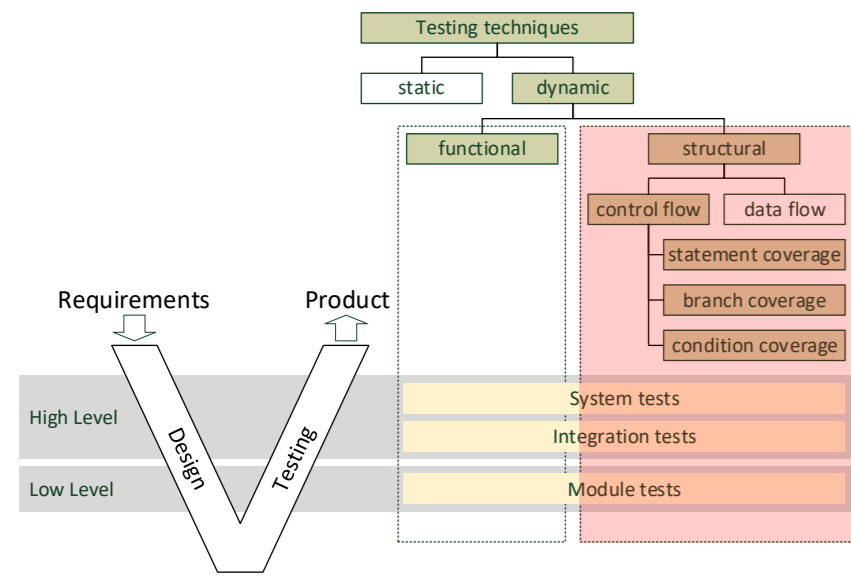
Targets:

- Infineon Aurix™ (TC2xx & TC3xx),
- Arm® Cortex® -A9,
- Intel® x86 (Atom® E3950),
- NXP QorIQ® P- and T-series,
- Arm® Cortex® -A5x under development

12			<code>// Compute n-th Fibonacci number using recursion.</code>
13			<code>// - n < 2 does not trigger the else branch.</code>
14		275	<code>unsigned fib(unsigned const n) {</code>
15	[+,+]	275	<code>return (n < 2)? n : fib(n-2) + fib(n-1);</code>
16		275	<code>}</code>
17			<code>// Unfold Collatz sequence and return its length.</code>
18			<code>// - n <= 1 will not execute the while loop at all.</code>
19			<code>// - n = 2^k will never trigger the 3*n+1 path.</code>
20		9	<code>unsigned collatz_depth(unsigned n) {</code>
21		9	<code>unsigned depth = 0;</code>
22	[+,+]	70	<code>while(n > 1) {</code>
		70	<code>10062C: e51b3010 ldr r3, [fp, #-16]</code>
		70	<code>100630: e3530001 cmp r3, #1</code>
	[+,+]	70	<code>100634: 9a000010 bls 10067c <_Z13collatz_depthj+0x68></code>
		61	<code>100678: eaffffeb b 10062c <_Z13collatz_depthj+0x18></code>
23	[+,+]	61	<code>n = (n&1)? 3*n+1 : n/2;</code>
		61	<code>100638: e51b3010 ldr r3, [fp, #-16]</code>
		61	<code>10063C: e2033001 and r3, r3, #1</code>
		61	<code>100640: e3530000 cmp r3, #0</code>
	[+,+]	61	<code>100644: 0a000005 beq 100660 <_Z13collatz_depthj+0x4c></code>
		16	<code>100648: e51b2010 ldr r2, [fp, #-16]</code>
		16	<code>10064C: e1a03002 mov r3, r2</code>
		16	<code>100650: e1a03083 lsl r3, r3, #1</code>
		16	<code>100654: e0833002 add r3, r3, r2</code>
		16	<code>100658: e2833001 add r3, r3, #1</code>
		16	<code>10065C: ea000001 b 100668 <_Z13collatz_depthj+0x54></code>
		45	<code>100660: e51b3010 ldr r3, [fp, #-16]</code>
		45	<code>100664: e1a030a3 lsr r3, r3, #1</code>
		61	<code>100668: e50b3010 str r3, [fp, #-16]</code>
24		61	<code>depth++;</code>
25			<code>}</code>
26		9	<code>return depth;</code>
27		9	<code>}</code>



High-level Structural Tests



Continuous and non-intrusive

- Statement Coverage
 - Branch Coverage (EX/NEX)
 - Performance measurement (count executed instructions)
- Measured on **object code level**
 - Measured on **release code**
 - **No instrumentation**
 - **No limitation due to trace buffer size**

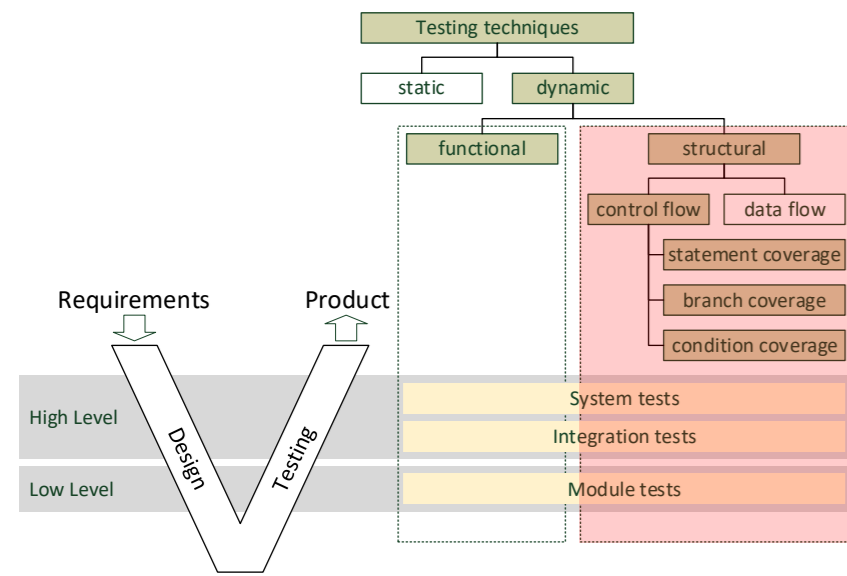
Targets:

- Infineon Aurix™ (TC2xx & TC3xx),
- Arm® Cortex® -A9,
- Intel® x86 (Atom® E3950),
- NXP QorIQ® P- and T-series,
- Arm® Cortex® -A5x under development.

▶	12		// Compute n-th Fibonacci number using recursion.
	13		// - n < 2 does not trigger the else branch.
▶	14	275	unsigned fib(unsigned const n) {
▶	15	[+,+] 275	return (n < 2)? n : fib(n-2) + fib(n-1);
▶	16	275	}
	17		// Unfold Collatz sequence and return its length.
	18		// - n <= 1 will not execute the while loop at all.
	19		// - n = 2^k will never trigger the 3*n+1 path.
▶	20	9	unsigned collatz_depth(unsigned n) {
▶	21	9	unsigned depth = 0;
▶	22	[+,+] 70	while(n > 1) {
▶	23	[+,+] 61	n = (n&1)? 3*n+1 : n/2;
▶	24	61	depth++;
	25		}
▶	26	9	return depth;
▶	27	9	}

High-level Structural Tests

Substitution of Low-Level Structural Tests



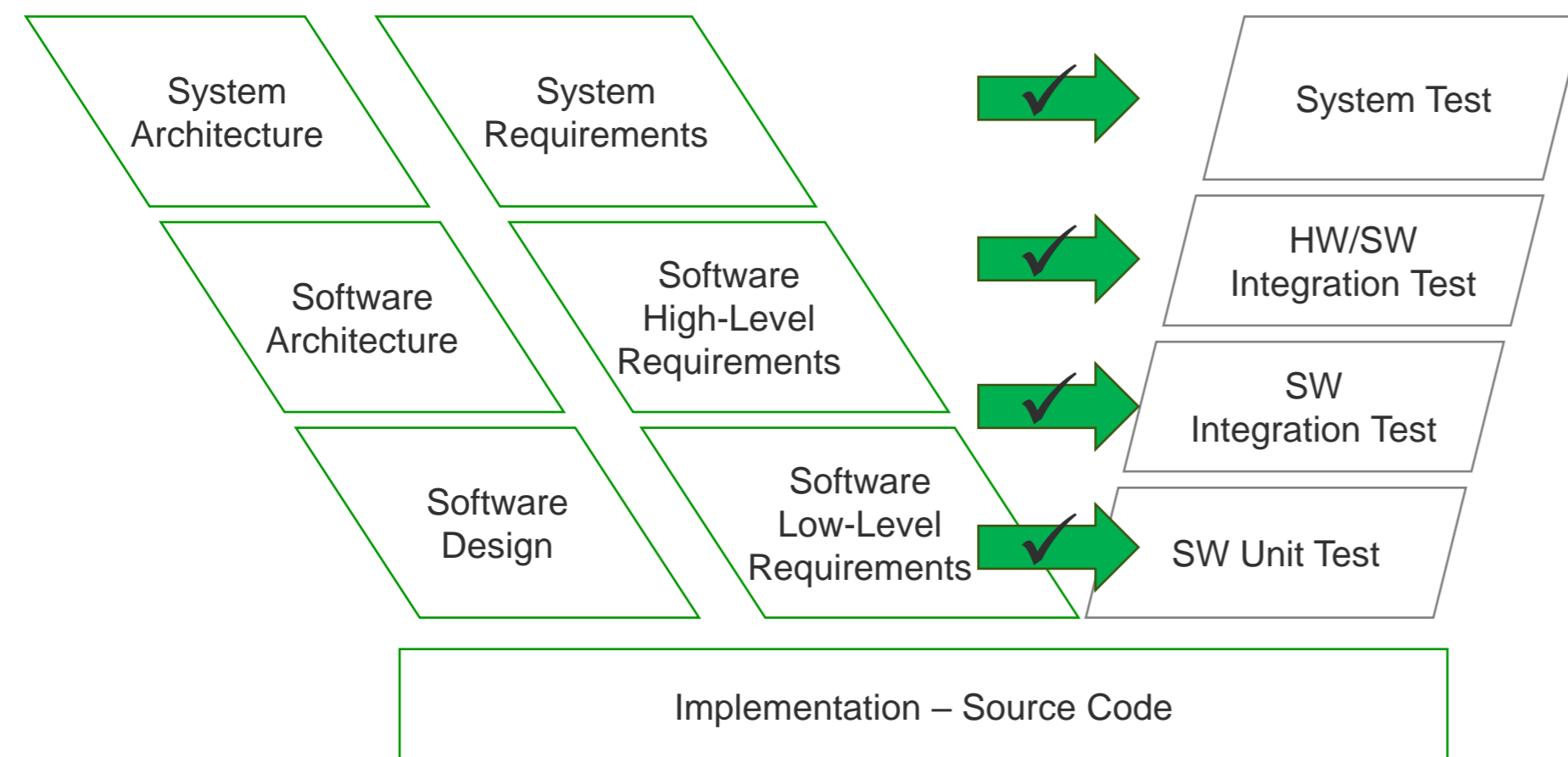
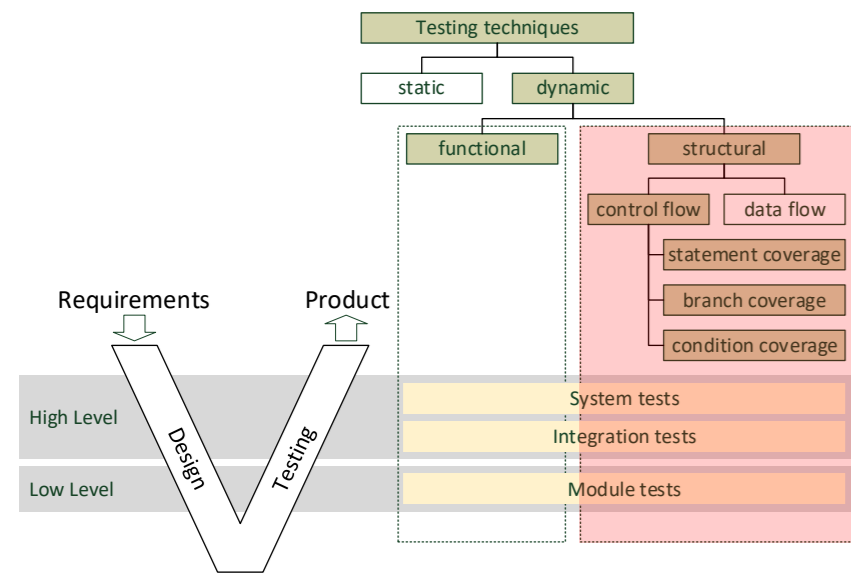
DO178C (6.4):

- If a test case and its corresponding test procedure are developed and executed for HW/SW or SW integration testing and satisfy the requirements-based coverage and structural coverage, it is not necessary to duplicate the test for low-level testing.
- Substituting nominally equivalent low-level tests for high-level tests may be less effective due to the reduced amount of overall functionality tested.

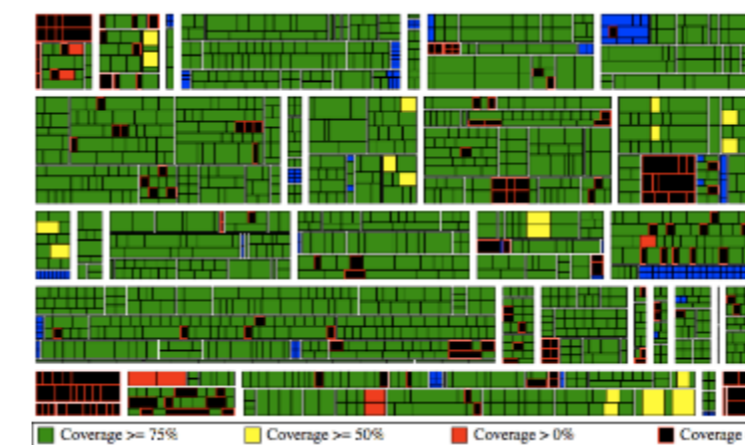


High-level Structural Tests

Substitution of Low-Level Structural Tests



Structural code coverage measured at high level tests: ~60%



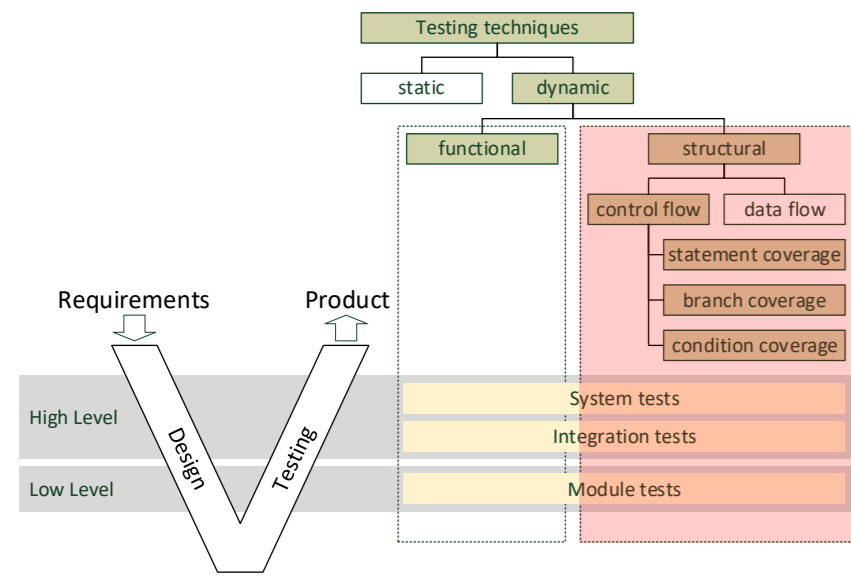
Structural coverage

SAVING

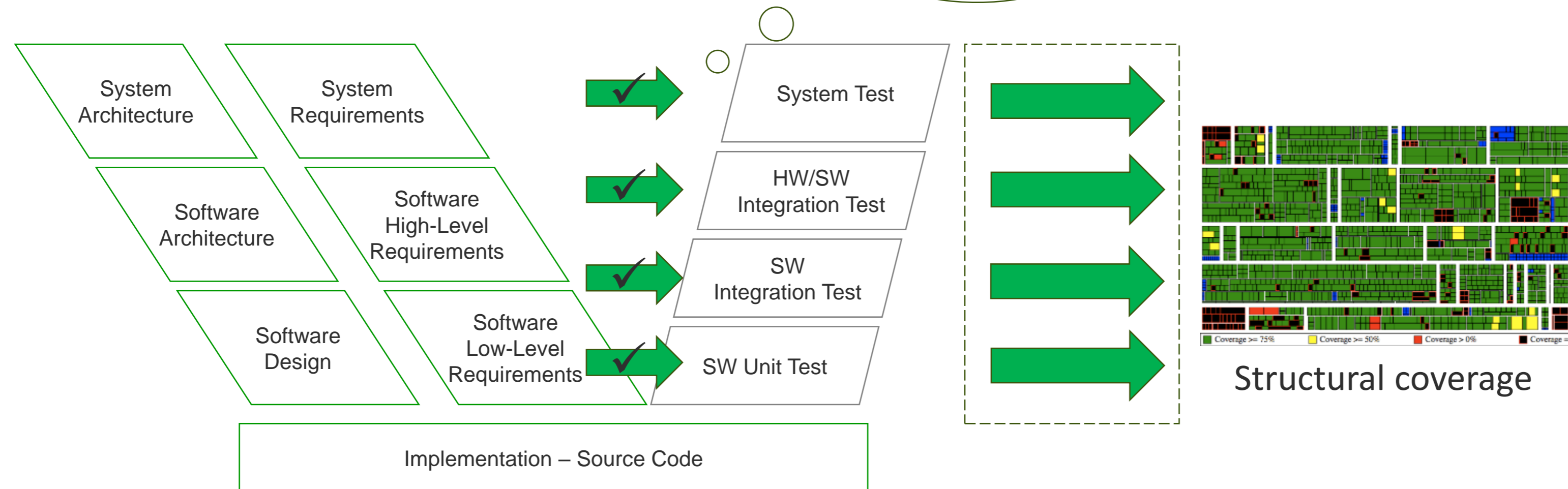
Remaining structural code coverage to be evidenced for certifications: ~ (95% - 60% = 35%)

High-level Structural Tests

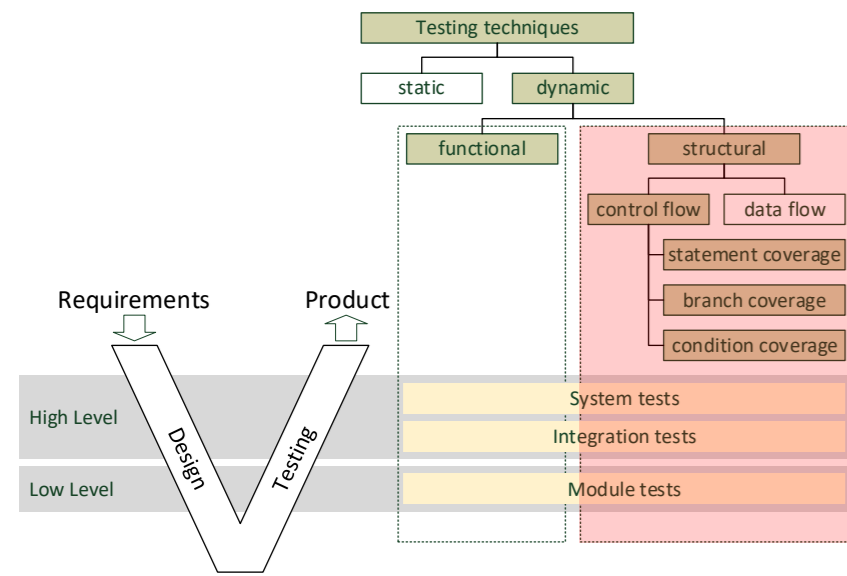
Completeness of High-Level Tests



Measurable statement of the completeness of High-Level Tests



High-level Structural Tests at Object Code Level



PROs

- It can demonstrate full code coverage at the object code level.
- It can support more “valid” coverage.
- It is closer to the final software .
- It can be implemented with source code programming language independence.
- It can reduce time-consuming manual analysis.
- No instrumentation is required.
- It can also be used for the objective measurement of the quality of integration and system tests.
- It can reduce the test effort by substituting low-level tests.
- Incomplete requirements and tests are found at the system level.

Listing 1: Illustrative example, source code in C

```
1 char* pass_fail(char grade) {
2     static char msg[2][5] = {"pass", "fail"};
3     int pass;
4     if (grade=='d' || grade=='f') {
5         pass = 0;
6     } else if (grade=='a' || grade=='b' ||
7               grade=='c') {
8         pass = 1;
9     } else { pass = -1; }
10    return pass ? msg[pass] : msg[0];
11 }
```

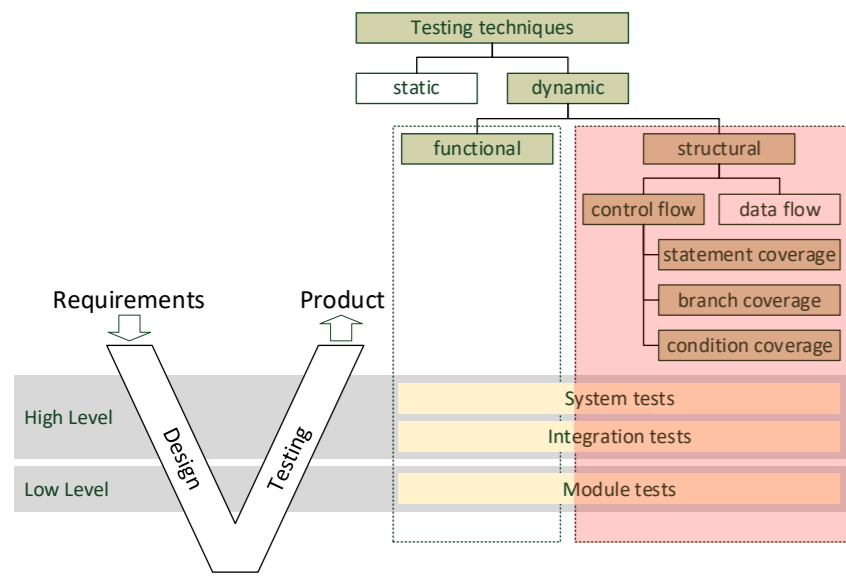
Listing 2: x86 code compiled with -O0

```
1 /* if (grade == 'd' || grade == 'f') */
2 8048439: cmpb  $0x64,-0x14(%ebp)
3 804843d: je    8048445 // jump if grade=='d'
4 804843f: cmpb  $0x66,-0x14(%ebp)
5 8048443: jne   804844e // jump if grade!='f'
6 8048445: movl  $0x0,-0x4(%ebp) // pass:=0
7 804844c: jmp   8048470 // jump to return
8 /* else if (grade=='a' || ... || grade=='c') */
9 804844e: cmpb  $0x61,-0x14(%ebp)
10 8048452: je    8048460 //jump if grade=='a'
11 8048454: cmpb  $0x62,-0x14(%ebp)
12 8048458: je    8048460 //jump if grade=='b'
13 804845a: cmpb  $0x63,-0x14(%ebp)
14 804845e: jne   8048469 //jump if grade!='c'
15 8048460: movl  $0x1,-0x4(%ebp) // pass:=1
16 8048467: jmp   8048470
17 /* else (pass:=-1) */
18 8048469: movl  $0xffffffff,-0x4(%ebp)
19 ...
```

T. Byun, V. Sharma, S. Rayadurgam, S. McCamant, and M. P. Heimdahl, 'Toward Rigorous Object-Code Coverage Criteria', in 2017 IEEE 28th International Symposium on Software Reliability Engineering (ISSRE), 2018, vol. 00, pp. 328–338.



High-level Structural Tests at Object Code Level



CONs

- Source code to object code traceability can be difficult (depending on compiler support).
- Optimizing compiler can use difficult-to-monitor flags to process multi-conditions. (we are working on solutions...)
- Typical tools use the source code level.

Listing 1: Illustrative example, source code in C

```

1 char* pass_fail(char grade) {
2     static char msg[2][5] = {"pass", "fail"};
3     int pass;
4     if (grade=='d' || grade=='f') {
5         pass = 0;
6     } else if (grade=='a' || grade=='b' ||
7               grade=='c') {
8         pass = 1;
9     } else { pass = -1; }
10    return pass ? msg[pass] : msg[0];
11 }

```

Listing 3: x86 code compiled with -O3

```

1 8048455: push %ebp
2 8048456: mov $0x804a01c,%eax // %eax:=msg[0]
3 804845b: mov %esp,%ebp
4 804845d: mov 0x8(%ebp),%edx // %edx:=grade
5 /* if (grade == 'd' || grade == 'f') */
6 8048460: mov %dl,%cl // %cl:=grade
7 // ASCII('d')=0x64, ASCII('f')=0x66,
8 // 'f'^0xffffd='d', 'd'^0xffffd='d'
9 8048462: and $0xffffffd,%ecx
10 8048465: cmp $0x64,%cl // 'd', grade
11 8048468: je 804847e // %cl=='d'->return
12 /* else if (grade=='a' || ... || grade=='c') */
13 /* else */
14 804846a: sub $0x61,%edx // %edx=grade-'a'
15 804846d: cmp $0x3,%dl // CF=%edx<3?1:0
16 8048470: sbb %eax,%eax // %eax:=CF?-1:0
17 8048472: and $0x2,%eax // %eax:=CF?2:0
18 8048475: dec %eax // %eax:=CF?1:-1
19 /* return pass ? msg[pass] : msg[0]; */
20 // %eax:=5*%eax
21 8048476: imul $0x5,%eax,%eax
22 // %eax:=msg+%eax
23 8048479: add $0x804a01c,%eax
24 804847e: ...

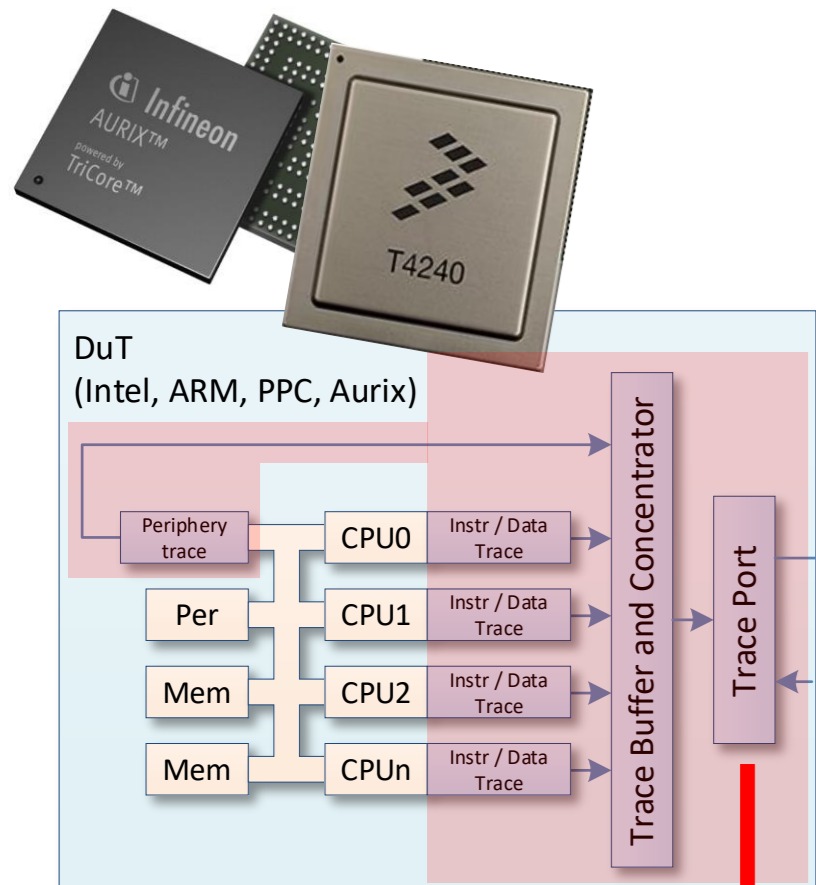
```

T. Byun, V. Sharma, S. Rayadurgam, S. McCamant, and M. P. Heimdahl, 'Toward Rigorous Object-Code Coverage Criteria', in 2017 IEEE 28th International Symposium on Software Reliability Engineering (ISSRE), 2018, vol. 00, pp. 328-338.



High-level Structural Tests

Key enabler: Processor Trace



Most processors provide trace infrastructure:

- [ARM Cortex-A/-M/-R](#): CoreSight architecture
- [Intel x86](#): IntelPT
- [NXP QorIQ P-series, T-series](#): Debug Assist Module
- [Infineon Aurix](#): Emulation Device

Trace data consists of high-bandwidth information for reconstruction of

- Control flow,
- OS related events (task changes),
- Data access (address, value),
and hardware-supported instrumentation: printf() replacement by simple MOV command.

Hardware-based monitoring infrastructure is integrated in most processors –
and is already paid by you ...

Mind trace interface access opportunities:

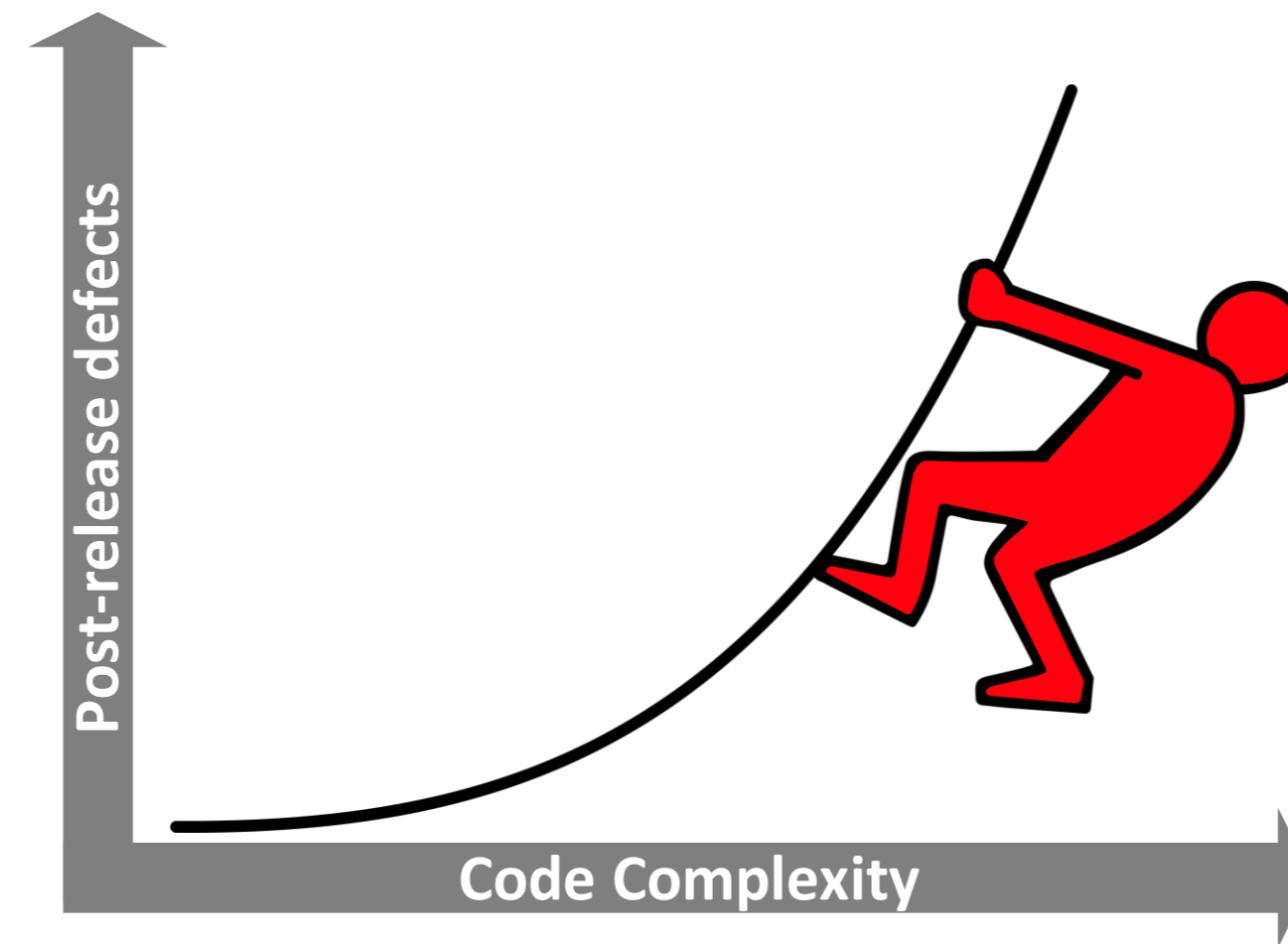
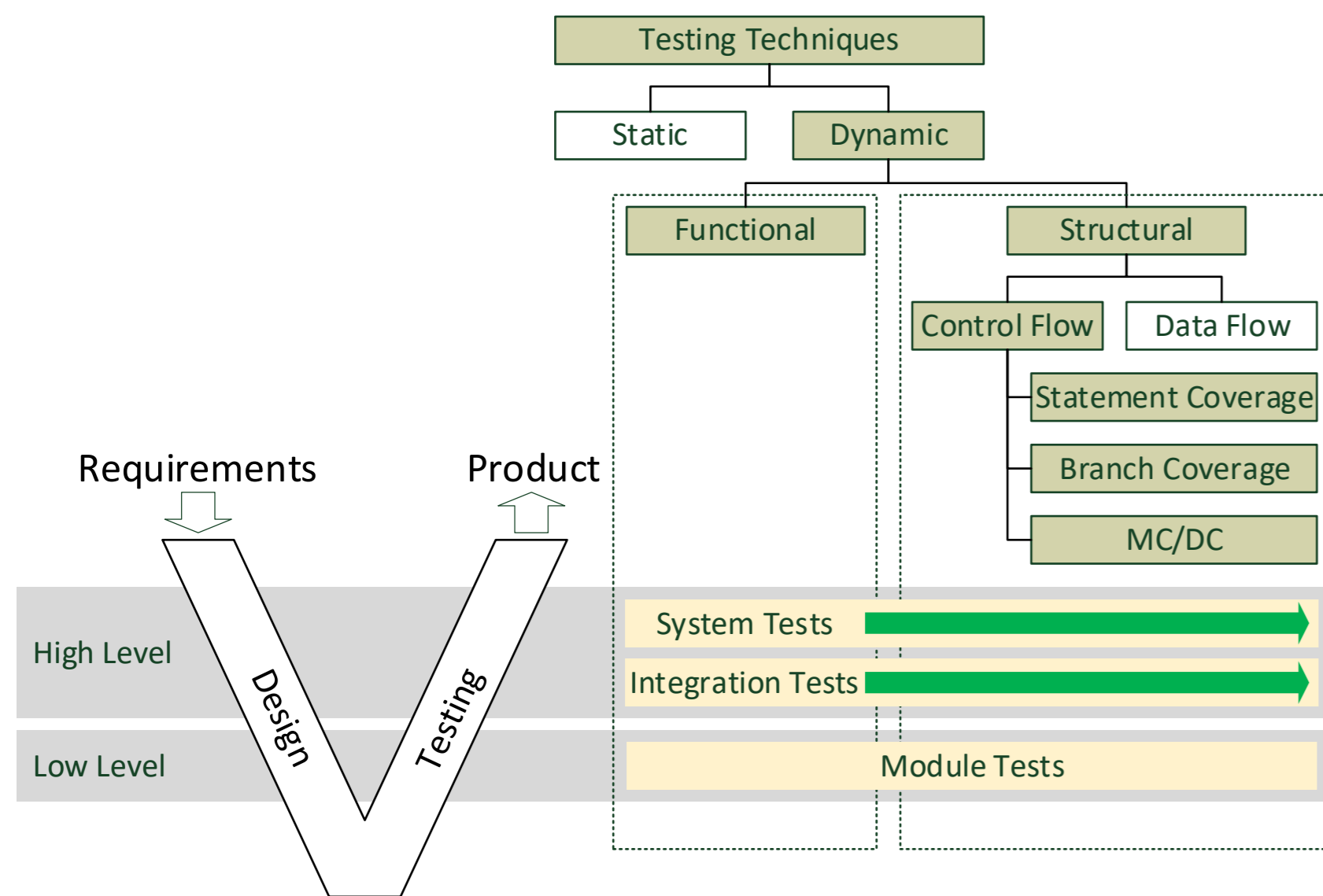
- in your hardware system requirement specifications and
- in your SoC architecture decision!

ARM® CoreSight®
Architecture Specification
Intel® 64 and IA-32 Architectures
Software Developer's Manual
T4240R2 Advanced QorIQ Debug
and Performance Monitoring
Reference Manual

TC29/7/6/3xED
32-Bit Single-Chip Microcontroller

Bug-free Software is a Myth.

But there's something we can do.



Contact:

Accemic Technologies GmbH

Franz-Huber-Str. 39

83088 Kiefersfelden

www.accemic.com

Dr.-Ing. Alexander Weiss

aweiss@accemic.com

+49 8033 6039795



ACCEMIC
TECHNOLOGIES

The pioneer in embedded systems dynamic analysis.
Automated, non-intrusive and continuous.

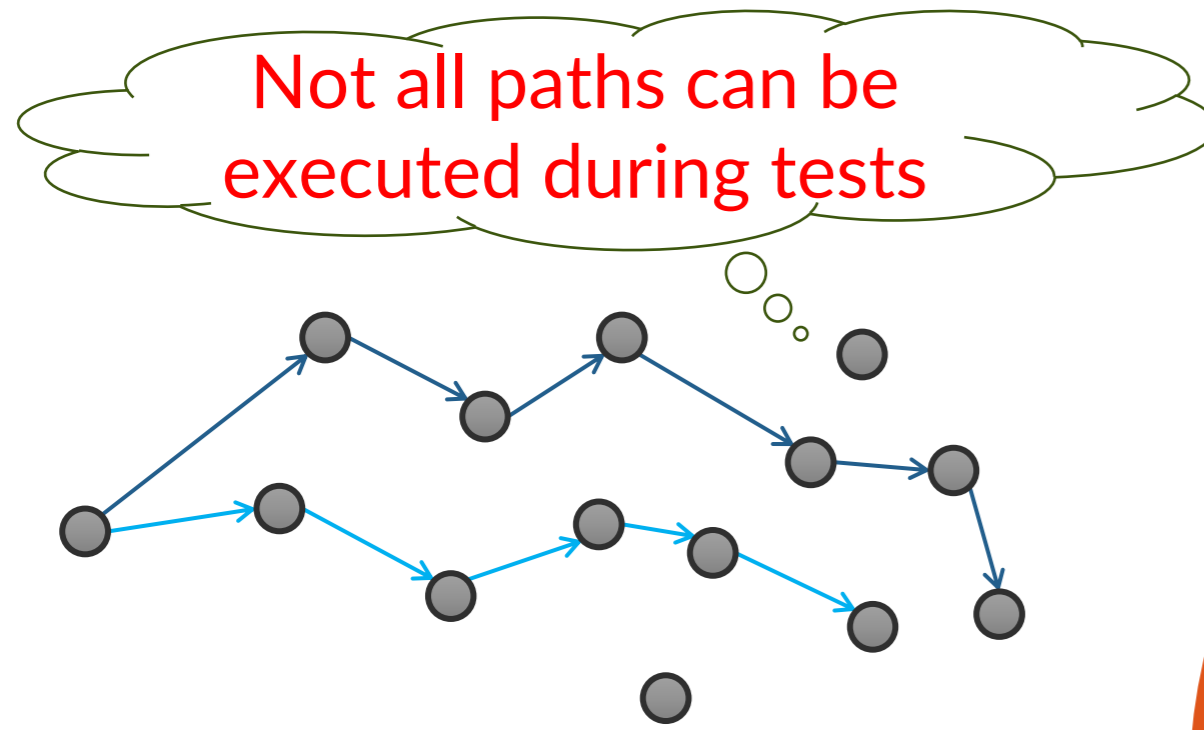
Backup slides



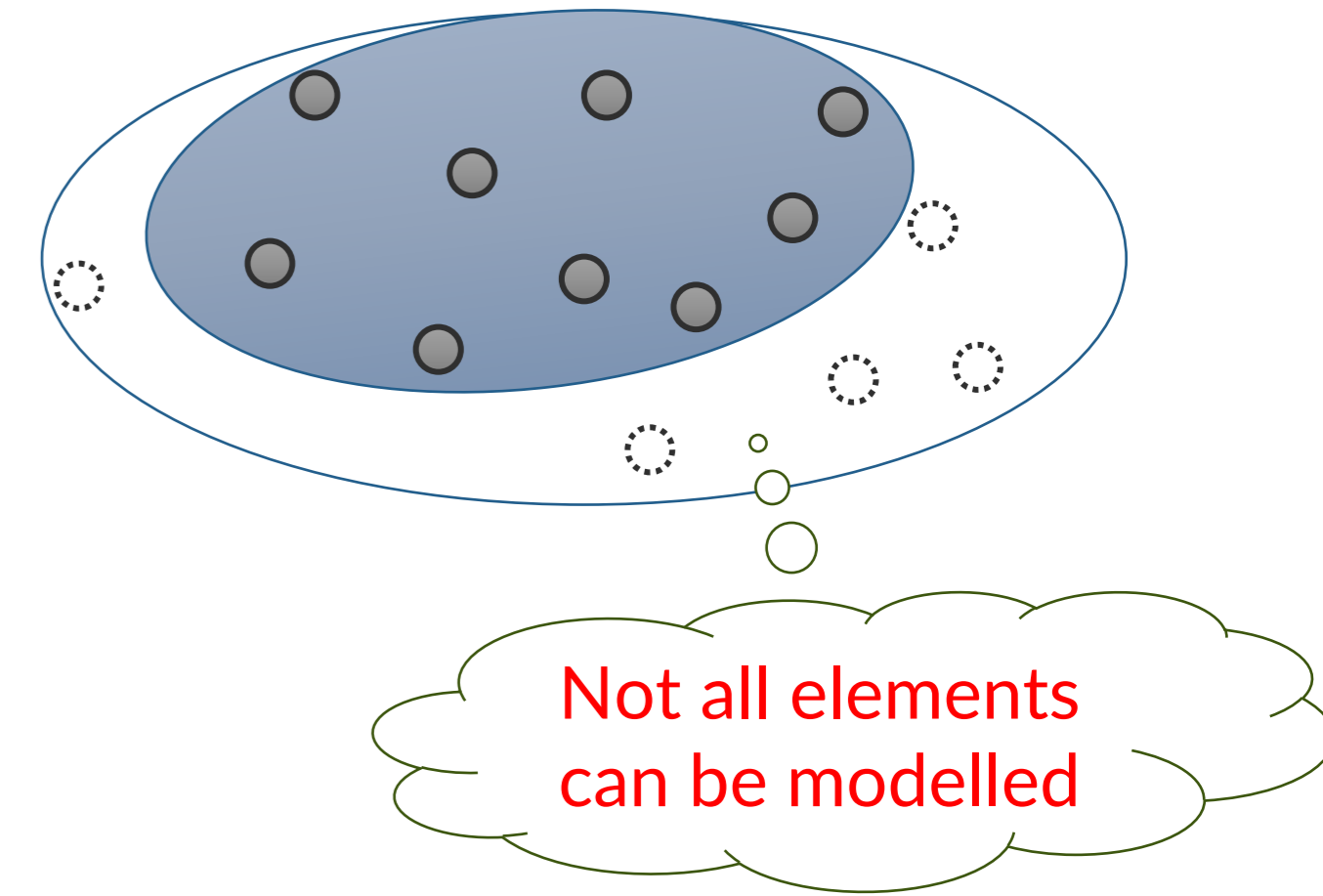
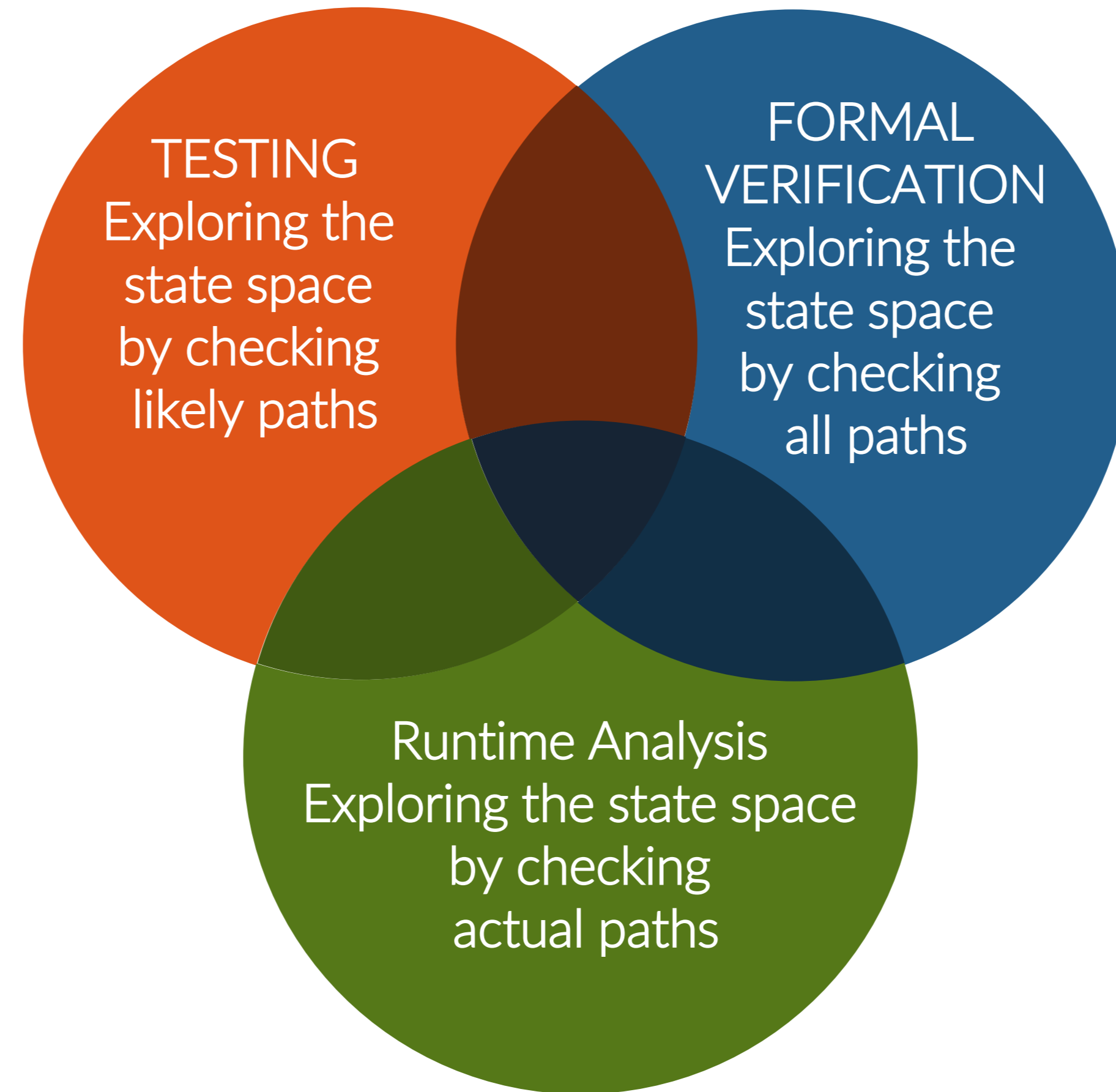
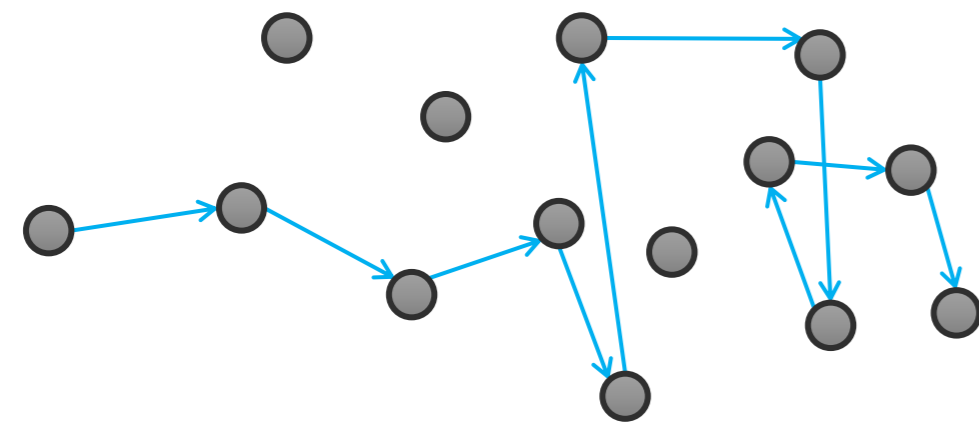
The pioneer in embedded systems dynamic analysis.
Automated, non-intrusive and continuous.

Runtime Analysis

before deployment

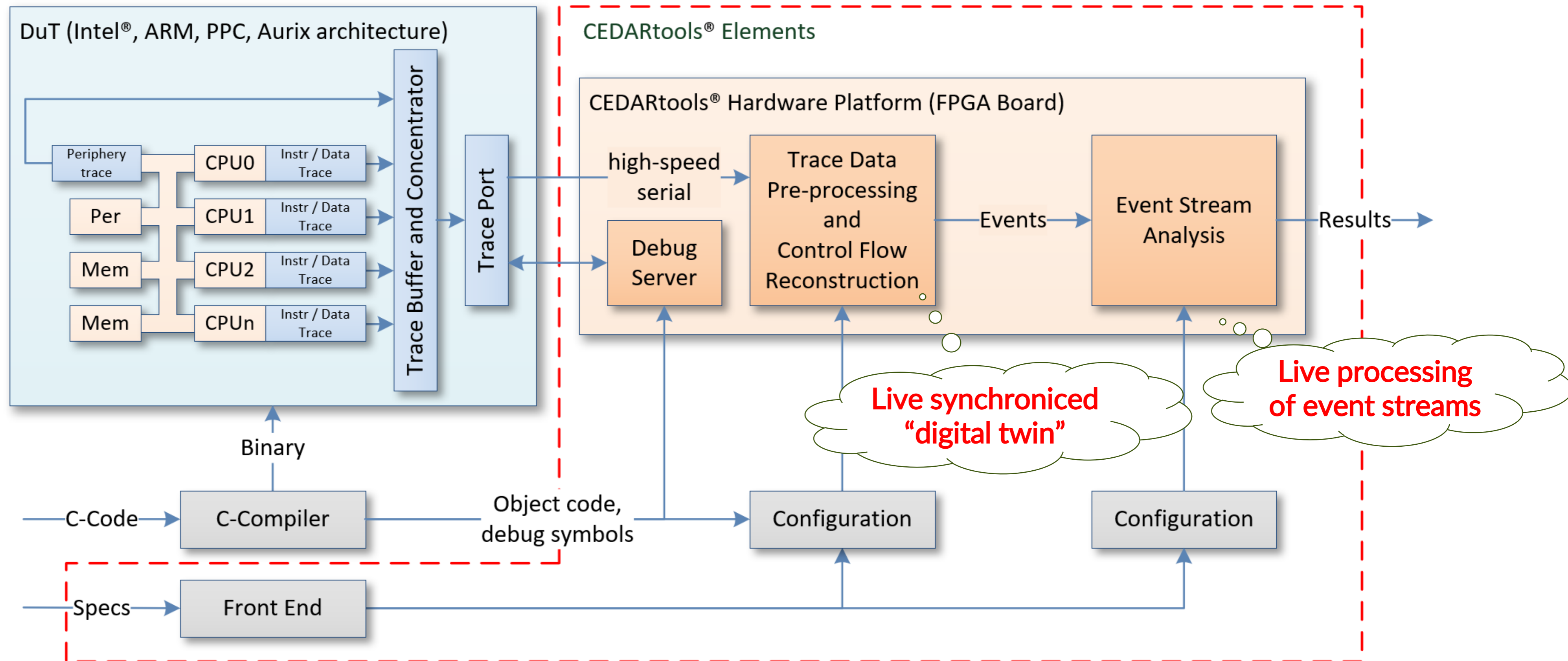
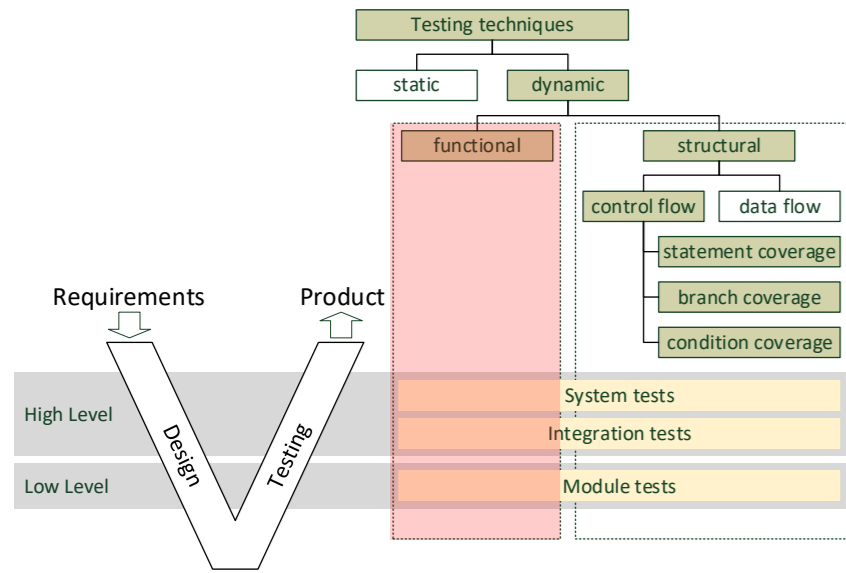


in deployment



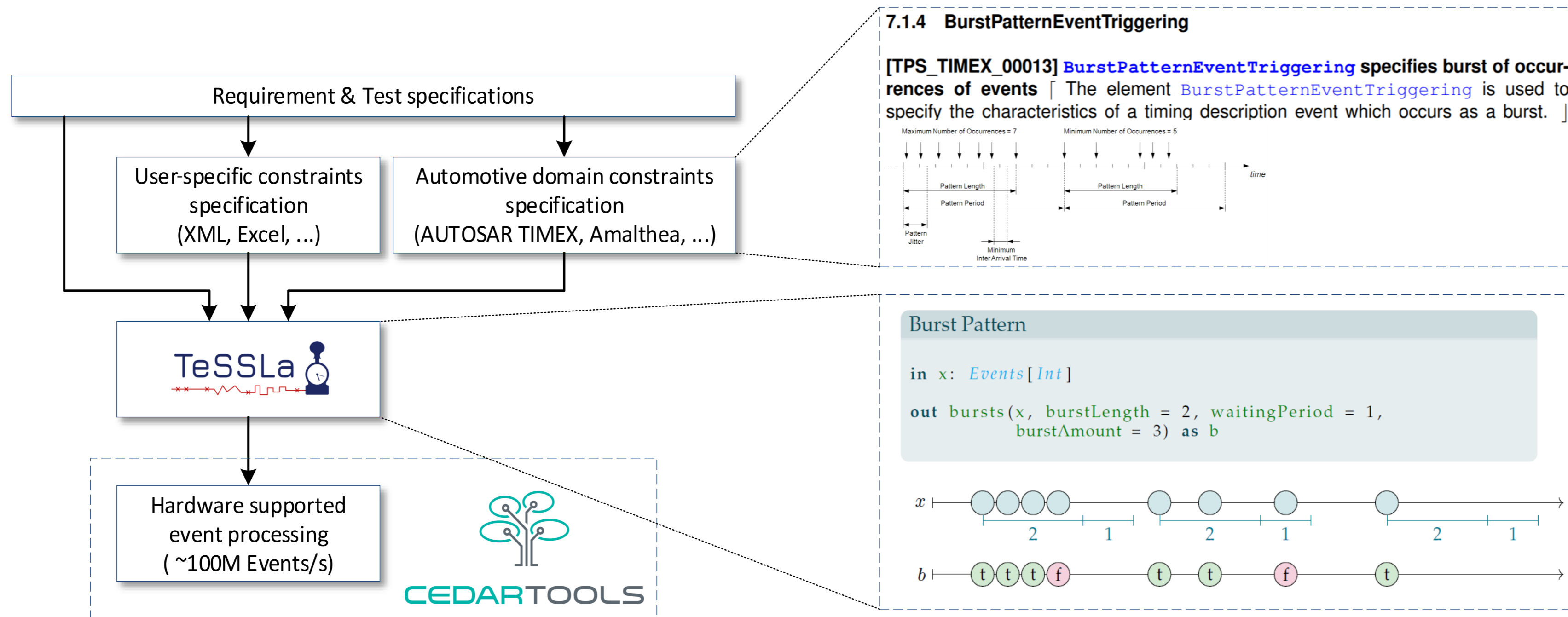
Runtime Analysis

Timing Analysis



Runtime Analysis

Timing Analysis



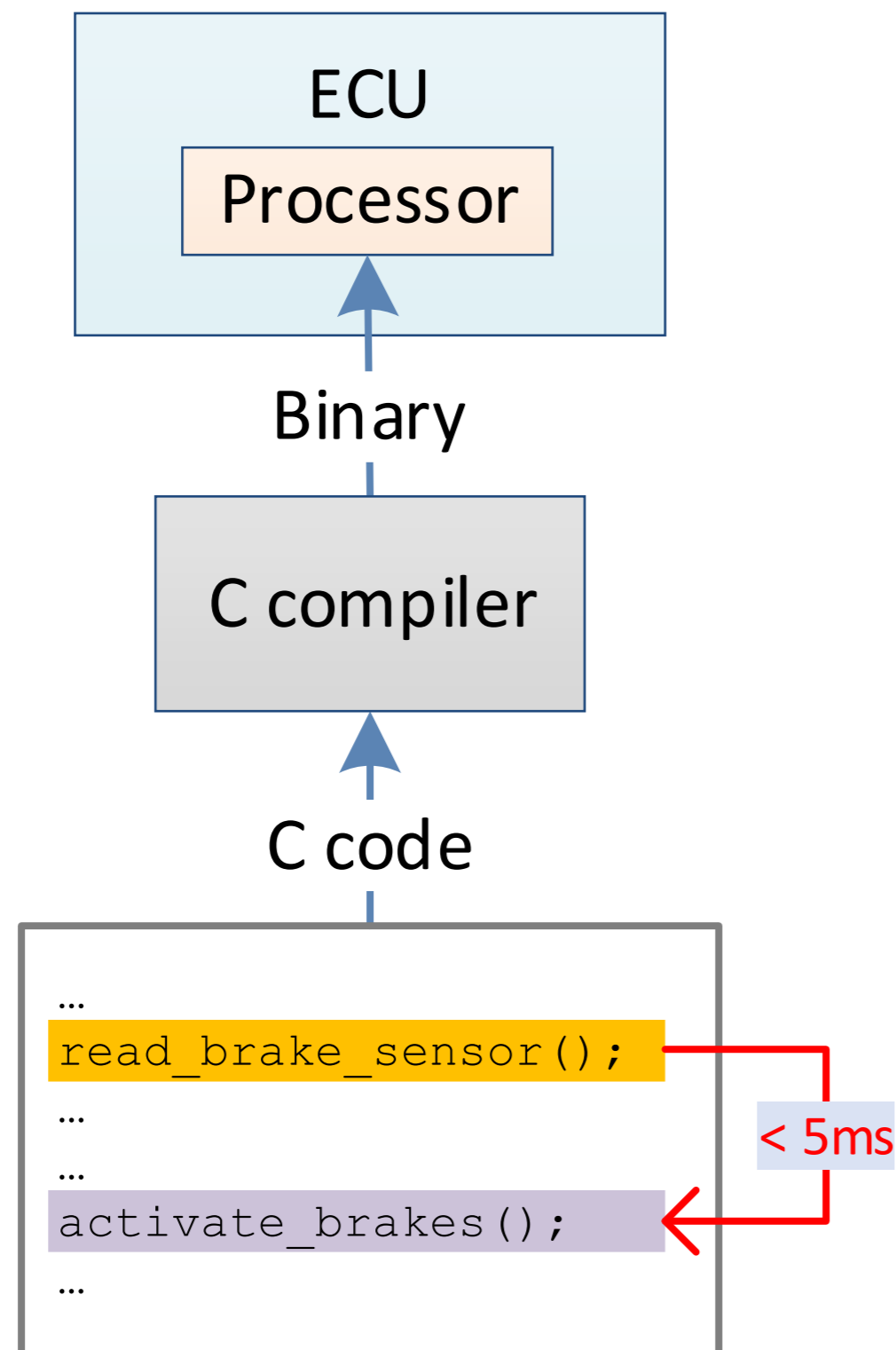
- High-level specification language
- Hardware-supported event processing
- Multiple constraints can be checked in parallel



(see tessla.io)

Runtime Analysis

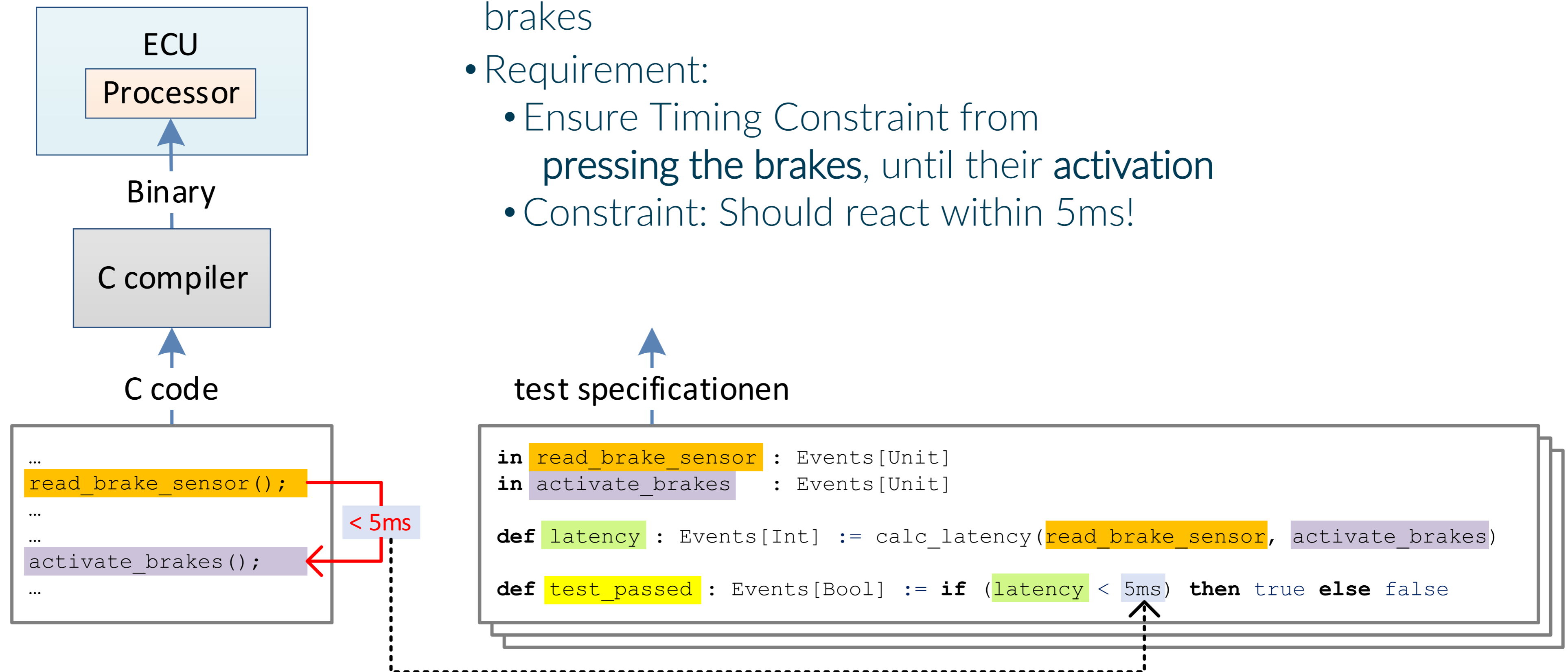
Timing Analysis



- Use case: Safety-critical application to control brakes
- Requirement:
 - Ensure Timing Constraint from **pressing the brakes**, until their **activation**
 - Constraint: Should react within 5ms!

Runtime Analysis

Timing Analysis

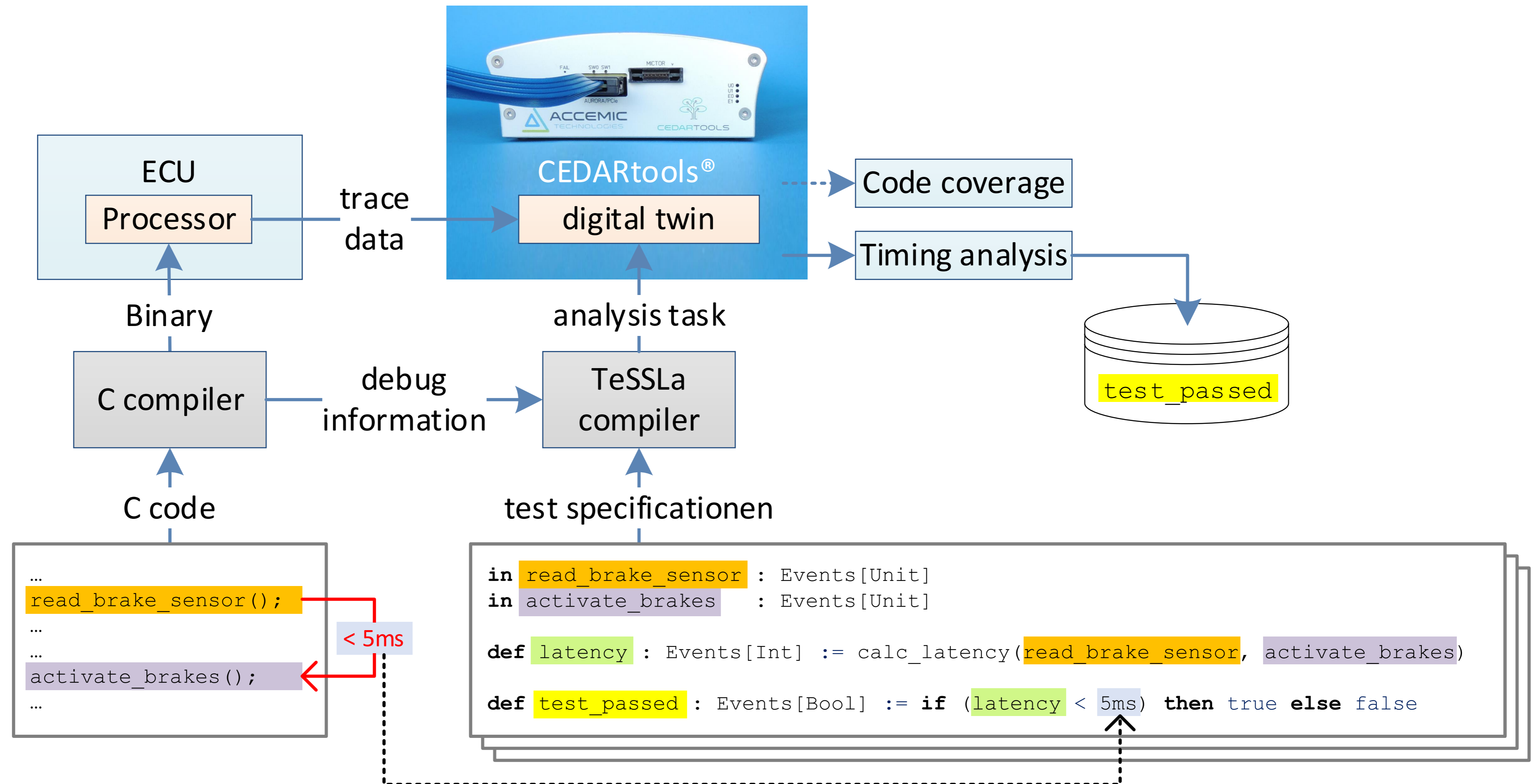


- Use case: Safety-critical application to control brakes
- Requirement:
 - Ensure Timing Constraint from **pressing the brakes**, until their **activation**
 - Constraint: Should react within 5ms!



Runtime Analysis

Timing Analysis



Runtime Analysis

Timing Analysis

<https://www.youtube.com/watch?v=3AYVWK-X9nw&feature=youtu.be>

```
File Edit Selection View Go Run Terminal Help
demo.cpp x latency-activate-brakes.tesla
demo > demo.cpp > main(int, char * [])
21
22 /* Program Entry */
23 int main(int argc, char *argv[])
24 {
25     /* Trace Setup */
26     atexit(cedar_kill_trace);
27     signal(SIGINT, sigint_handler);
28     cedar_linux_init_epu(false);
29     cedar_set_appid(0);
30
31     /* Program Routine */
32     while(1) {
33         run_task();
34         usleep(10e3);
35     }
36
37     return 0;
38 }
39
40 void run_task()
41 {
42     /* Sample Brake Sensor */
43     float brake_angle = read_brake_sensor();
44
45     /* Process */
46     int strength;
47     strength = calculate_brake_strength_for_angle(brake_angle);
48 }
```

